

Interfacing to High Speed ADCs via SPI

by the High Speed Converter Division

INTRODUCTION

This application note describes how to use the SPI port on Analog Devices, Inc., high speed converters. In addition, this application note defines the electrical, timing, and procedural requirements for interfacing to these devices. The implementation is compatible with industry-standard SPI ports and employs, at minimum, a 2-wire mode and optional chip select.

DEFINITION

The SPI port consists of three pins: the serial clock pin (SCLK), the serial data input/output pin (SDIO), and the chip select bar pin (CSB). Optionally, some chips may implement a serial data out pin (SDO), which is referred to as 3-wire mode. To minimize pin count, most chips omit this pin. However, if it is included, it is used only for reading data from the device.

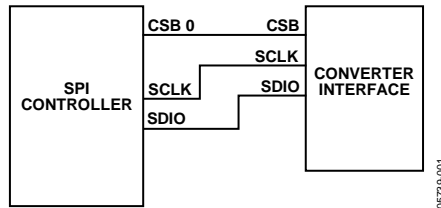


Figure 1. Single Device Control in 2-Wire Mode

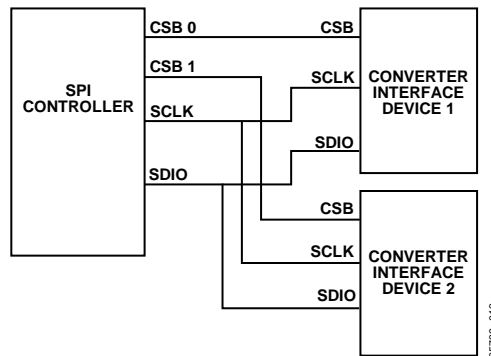


Figure 2. Multiple Device Control in 2-Wire Mode

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REVISION HISTORY

4/07— Initial Version to Rev. A

| | |
|--|-----------|
| Updated Format..... | Universal |
| Changes to Transfer Register Section | 8 |
| Changes to Figure 13..... | 10 |
| Added Table 6..... | 11 |
| Added PLL Control (0x00A) Section..... | 11 |
| Changes to Table 8..... | 12 |

12/05— Revision 0: Initial Version

| Address ¹ and Parameter Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value ¹ | Comments |
|---|---|------------|---|---------------|--------------------------------------|---|---|-------------------|----------------------------|---|
| 14–output_mode | 0: Level Option 0 1: Level Option 1 2: Level Option 2 3: Level Option 3 | | Output mux enable (interleave) | Output enable | DDR enable | Output invert | 0: Offset binary 1: Twos complement 2: Gray code 3: Reserved | | device specific | Configures the outputs and the format of the data. |
| 15–output_adjust | Output driver termination; Bits[7:4] | | | | Output driver current; Bits[3:0] | | | | device specific | Determines LVDS or other output properties. Primarily functions to set the LVDS span and common-mode levels in place of an external resistor. |
| 16–output_phase | Output polarity | | | | Output clock phase adjust; Bits[3:0] | | | | 00h | On devices that utilize clock divide, determines which phase of the divider output is used to supply the output clock. Internal latching is unaffected. |
| 17–output_delay | Enable | DLL Enable | 6-bit output delay; Bits[5:0] | | | | | | 00h | This sets the fine output delay of the output clock but does not change internal timing. |
| 18–vref | V _{REF} Select 0: Primary (0) 1: Secondary (1) 2: Option 2 3: Option 3 | | 6-bit internal V _{REF} adjustment; Bits[5:0] | | | | | | 20h | Select and/or adjust the V _{REF} . |
| 19–user_patt1_lsb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 00h | User-Defined Pattern 1 LSB. |
| 1A–user_patt1_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 00h | User-Defined Pattern 1 MSB. |
| 1B–user_patt2_lsb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 00h | User-Defined Pattern 2 LSB. |
| 1C–user_patt2_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 00h | User-Defined Pattern 2 MSB. |
| 1D–user_patt3_lsb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 00h | User-Defined Pattern 3 LSB. |
| 1E–user_patt3_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 00h | User-Defined Pattern 3 MSB. |
| 1F–user_patt4_lsb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 00h | User-Defined Pattern 4 LSB. |
| 20–user_patt4_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 00h | User-Defined Pattern 4 MSB. |
| 21–serial_control | LSB first | | | | PLL optimize | 000: Normal bit stream 001: 8 bits 010: 10 bits 011: 12 bits 100: 14 bits 101: 16 bits | | | 00h | Serial stream control. Default causes MSB first and the native bit stream. |
| 22–serial_ch_stat | | | | | | | Ch output reset | Ch power-down | 00h | Used to power down individual sections of a converter(local). |
| 24–misr_lsb | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 00h | Least significant byte of MISR (read-only). |
| 25–misr_msb | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 00h | Most significant byte of MISR (read-only). |
| 2A–features | | | | | | | OVR alternate pin | OVR output enable | 00h | Auxiliary feature set control. |
| 2B–high pass | | Tune | | | | Corner frequency Bit 0: DC Bit 1 to Bit 7: Alternate corner frequencies | | | 00h | High-pass filter control. |
| 2C–ain | | | | | | | | Input impedance | 00h | Analog input control. |
| 2D–cross_point | | | | | | | | | 00h | Analog input cross point switch. |
| FF–device_update | Enable HW transfer | | | | | | | SW transfer | 00h | Synchronously transfers data from the master shift register to the slave. |

¹ Hexadecimal.² Not supported on most devices.

