

Migrating from AT89C2051/C4051 to AT89LP2052/LP4052

New Features

- 20 MIPS throughput at 20 MHz Clock Frequency and 2.7V, 85° C Operating Conditions
- Single Clock Cycle per Byte Fetch
- Serial Interface for Program Downloading
- 32-byte Fast Page Programming Mode
- 256 x 8 Internal RAM
- 32-byte User Signature Array
- Configurable I/O with Quasi-bidirectional, Input, Push-pull Output, and Open-drain Modes
- Enhanced UART with Automatic Address Recognition and Framing Error Detection
- Enhanced SPI with Double-buffered Send/Receive
- Programmable Watchdog Timer with Software Reset
- 4-level Interrupt Priority
- Analog Comparator with Selectable Interrupt and Debouncing
- Two 16-bit Enhanced Timer/Counters with 8-bit PWM
- Brown-out Detector
- Power-off Flag
- Internal Power-on Reset
- Interrupt Recovery from Power-down Mode

1. Introduction

The purpose of this application note is to help users convert existing designs from AT89C2051/C4051 to AT89LP2052/LP4052. This application note describes AT89LP2052/LP4052 memory sizes, features, SFR mapping, and register differences. More detailed information can be found in the AT89LP2052/LP4052 datasheet.

2. Memory Sizes

Memory	AT89C2051	AT89C4051	AT89LP2052	AT89LP4052
Flash	2K Bytes	4K Bytes	2K Bytes	4K Bytes
RAM	128 Bytes	128 Bytes	256 Bytes	256 Bytes



Flash Microcontrollers

Application Note



3. Single Clock Cycle per Byte Fetch

The AT89LP2052/LP4052 is built around an enhanced CPU core that can fetch a single byte from memory every clock cycle.

4. Serial Interface for Program Downloading

The program memory can be programmed using the 4 SPI pins while RST is strapped to V_{CC} . Programming through the serial interface shares the same command format as programming through the parallel interface.

5. 32-byte Fast Page Programming Mode

Up to 32 bytes of data can be loaded to be written at any time. The Load Code Page Buffer command allows for interrupted loading of 32 bytes of data that can be written later. The Write Code Page command can write a previously loaded page of data or load and write anywhere from 1 to 32 bytes of data to code memory.

6. 32-byte User Signature Array

Thirty-two bytes are accessible to the user to program their own desired data. Bytes can be either programmed by parallel or serial mode.

7. Configurable I/O with Quasi-bidirectional, Input, Push-pull Output, and Open-drain Modes

All 15 port pins can be configured to one of four modes:

1. Quasi-bidirectional Output mode pins function similar to 8051 port pins.
2. Input-only Mode is a Schmitt-triggered input for improved noise rejection.
3. Open-drain Output configuration turns off all pull-ups and only drives the pull-down translator of the port pin when the port register contains a logic "0".
4. Push-pull Output configuration has the same pull-down structure as both the open-drain and quasi-bidirectional output modes, but provides a continuous strong pull-up when the port register contains a logic "1".

All port pins default to input-only mode after reset. Port modes may be assigned in software on a pin-by-pin basis.

8. Enhanced UART with Automatic Address Recognition and Framing Error Detection

When used for frame error detection, the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON Register. Automatic Address Recognition allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparison.

9. Enhanced SPI with Double-buffered Send/Receive

The enhanced SPI mode allows the write buffer to hold the next byte to be transmitted. As long as the CPU can keep the write buffer full, multiple bytes may be transferred with minimal latency between bytes.

10. Programmable Watchdog Timer with Software Reset

The watchdog timer allows control of the microcontroller to be regained in situations where the CPU may be subjected to software upsets. The watchdog timer is enabled by software and resets the microcontroller after a specified period, unless the firmware intervenes and services the watchdog before its timeout. The watchdog timer timeout period is user adjustable from 16K to 2048K clock cycles.

11. Four-level Interrupt Priority

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing a bit in the Interrupt Priority (IP) register and in the Interrupt Priority High (IPH) register.

12. Analog Comparator with Selectable Interrupt and Debouncing

When the positive input AIN0 (P1.0) is greater than the negative input AIN1 (P1.1), the logical output is 1, otherwise the output is 0. The comparator can be configured to cause an interrupt under a variety of output value conditions by setting the CM bits in ACSR in the SFR map. Three debouncing modes are provided to filter out noise caused by slow moving analog inputs.

13. Two 16-bit Enhanced Timer/Counters with 8-bit PWM

Timers count once every clock cycle compared to the AT89C2051/C4051 which count once every 12 clock cycles (one machine cycle). Timer 1 Mode 0 can act as a 9 to 16 bit timer/counter versus a 13-bit timer/counter for the AT89C2051/C4051.

For the 8-bit PWM a generated waveform is output on the Timer 1 input pin. Timer 0 acts as an 8-bit prescaler to select the Pulse-width Modulation base.

14. Brown-out Detector

When V_{CC} decreases to a value below the trigger level, the Brown-out Reset is immediately activated. The Brown-out Detection ensures the system will enter reset without the possibility of errors induced by incorrect execution if V_{CC} fails or dips.

15. Power-off Flag

The Power Off Flag is in the PCON register in the SFR map and is set to “1” during power up (i.e. cold reset). The Power-Off Flag is not affected by External Reset or Brown-Out Reset (i.e. warm resets) and can be used to indicate that the microcontroller has been powered down.

16. Internal Power-on Reset

When V_{CC} reaches the Power-on Reset threshold voltage an internal reset signal is generated. The Power-on Reset circuit ensures that the device is reset from power-on.

17. Interrupt Recovery from Power-down Mode

An enabled external interrupt (through INT0 or INT1) can be used to exit from the power-down mode. In older derivatives, the only way to recover from the power-down mode was to perform a hardware reset.

18. System Clock Out

When the System Clock out fuse is enabled, P3.7 will output the system clock with no divisions.

19. Parallel Programming Differences

All command and data bytes are input/output through Port 1 when P3.2 is pulled low and clocked in with a positive pulse on Xtal1. Other than pulsing Xtal1, no other clock is required. Older derivatives use Port 3 for control signals and Port 1 for data output.

Programming through the parallel interface shares the same command format as programming through the serial interface. Parallel programming requires the Program Enable command to be issued first before programming may begin.

20. SFRs Mapping

The highlighted SFR locations are new registers for the AT89LP2052/LP4052 devices.

0F8H									0FFH
0F0H	B								0F7H
0E8H									0EFH
0E0H	ACC								0E7H
0D8H									0DFH
0D0H	PSW					SPCR			0D7H
0C8H									0CFH
0C0H		P1M0	P1M1				P3M0	P3M1	0C7H
0B8H	IP	SADEN							0BFH
0B0H	P3							IPH	0B7H
0A8H	IE	SADDR	SPSR						0AFH
0A0H							WDRST	WDTCON	0A7H
98H	SCON	SBUF							9FH
90H	P1	TCONB	RL0	RL1	RH0	RH1		ACSR	97H
88H	TCON	TMOD	TL0	TL1	TH0	TH1			8FH
80H		SP	DPL	DPH			SPDR	PCON	87H

21. Register Differences

Registers and bits in AT89C2051/C4051 and AT89LP2052/LP4052 equivalents.

AT89C2051/C4051		AT89LP2052/LP4052	
Reg		Reg	
IE	EA -- -- ES ET1 EX1 ET0 EX0	IE	EA EC -- ES ET1 EX1 ET0 EX0
IP	-- -- -- PS PT1 PX1 PT0 PX0	IP	-- PC -- PS PT1 PX1 PT0 PX0
PCON	SMOD -- -- -- GF1 GF0 PD IDL	PCON	SMOD1 SMOD0 PWDEX POF GF1 GF0 PD IDL

22. Code Examples

22.1 Port Pin Configuration

The AT89LP2052/LP4052 port pins can be set to one of four modes. Following reset the port pins are defaulted to input only mode. To configure the port pins to behave like the traditional 8051 architecture users can insert the following code at the beginning of their program.

```
MOV 0C2H,#00H      ;Set P1M0 for quasi-bidirectional mode
MOV 0C3H,#00H      ;Set P1M1 for quasi-bidirectional mode
MOV 0C6H,#00H      ;Set P3M0 for quasi-bidirectional mode
MOV 0C7H,#00H      ;Set P3M1 for quasi-bidirectional mode
```

22.2 Timer Differences

Timers count once every clock cycle compared to the AT89C2051/C4051 which count once every 12 clock cycles (one machine cycle). Timer 1 Mode 0 can act as a 9 to 16 bit timer/counter versus a 13-bit timer/counter for the AT89C2051/C4051.

Code for AT89C2051/C4051

```
;;TEST TIMER0 & TIMER1
;;C2051/4051 TIMER INCREMENTS EVERY MACHINE CYCLE (12 clock cycles)
;;FOR LP2052/4052, EACH INSTRUCTION IS NOT THE SAME # OF CLOCK CYLES AS THE
;;C2051/4051

MOV TCON,#00H
MOV TMOD,#00H      ;BEGIN TIMER0 MOD0
MOV TL0,#01DH
MOV TH0,#0FFH
MOV TH1,#00H
MOV TL1,#00H
SETB TR0
NOP                ;+12 clock cycles
NOP                ;+12 clock cycles
NOP                ;+12 clock cycles
MOV R0,TCON        ;+24 clock cycles
CJNE R0,#30H,TIMERR ;+24 clock cycles
MOV A,TL0          ;+12 clock cycles, TL0 = 1DH + 8
CJNE A,#25H,TIMERR
```



Code for LP2052/4052

```

;;TEST TIMER0 & TIMER1
MOV TCON,#00H
MOV TMOD,#00H ;BEGIN TIMER0 MOD0
MOV TL0,#01DH
MOV TH0,#0FFH
MOV TH1,#00H
MOV TL1,#00H
SETB TR0
NOP ;+1 clock cycle
NOP ;+1 clock cycle
NOP ;+1 clock cycle
MOV R0,TCON ;+2 clock cycles
CJNE R0,#30H,TIMERR ;+4 clock cycles
MOV A,TL0 ;+2 clock cycles (only 1 clock cycle
;is counted by the timer) TL0 = 1DH + A
CJNE A,#27H,TIMERR

```

23. Serial Port Differences

The AT89LP2052/LP4052 only counts once every clock cycle versus once every 12 clock cycles in the old AT89C2051/4051 device. The baud rate generator must have different reload values for Timer 1 to generate the same baud rates as the old 8051 core.

Baud Rate	Fosc (MHz)	SMOD1	Timer 1			
			C/T	Mode	Reload Value (C2051/4051)	Reload Value (LP2052/4052)
Mode 2: 375K	12	0	X	X	X	X
62.5K	12	1	0	2	FFH	F4H
19.2K	11.059	1	0	2	FDH	DCH
9.6K	11.059	0	0	2	FDH	DCH
4.8K	11.059	0	0	2	FAH	B8H
2.4K	11.059	0	0	2	F4H	70H
1.2K	11.059	0	0	1	E8H	FEE0H
137.5	11.986	0	0	1	1DH	F55CH
110	6	0	0	1	72H	F958H
110	12	0	0	1	FEEBH	F304H

Below is sample code that sets up the UART.

```
ORG 00H
LJMP INIT

ORG 023H
JMP SER_INT

INIT:
MOV SCON,#40H           ;MODE #1, 8-BIT UART
MOV TMOD,#20H          ;TIMER1, MODE 2, 8-BIT AUTO RELOAD
MOV TH1,#Value         ;AUTO RELOAD Value
MOV TCON,#40H          ;SET TIMER1

MOV IE,#90H            ;SERIAL INTERRUPT
CLR TI
MOV SBUF,#0AAH

LOOP:
SJMP LOOP

SER_INT:
CLR TI
MOV P1,SBUF
MOV SBUF,#0AAH
RETI

END
```



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