

NPN power transistor
Features

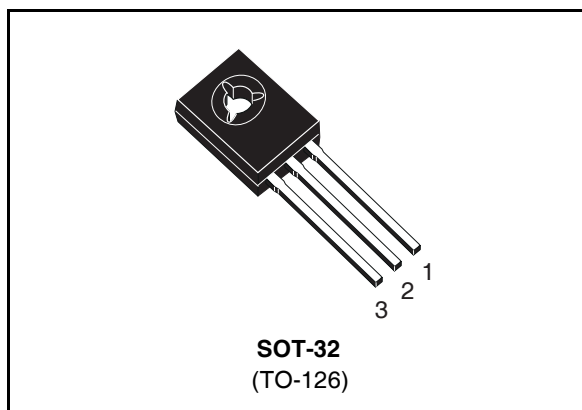
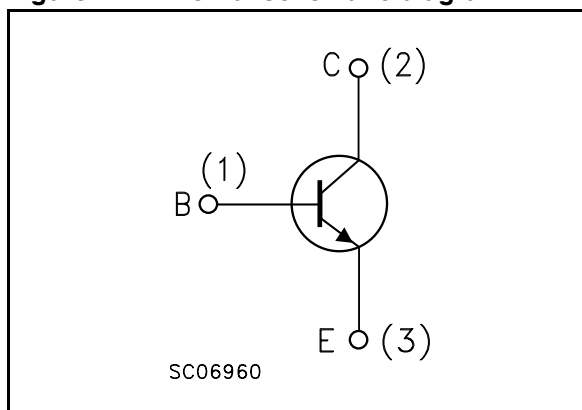
- NPN transistor

Applications

- General purpose switching

Description

The device is manufactured in Planar technology with "Base Island" layout. The resulting transistor shows exceptional high gain performance coupled with very low saturation voltage.


Figure 1. Internal schematic diagram

Table 1. Device summary

Order code	Marking	Package	Packaging
BD179	BD179	SOT-32	Tube

1 Electrical ratings

Table 2. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-base voltage ($I_E = 0$)	80	V
V_{CEO}	Collector-base voltage ($I_B = 0$)	80	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	5	V
I_C	Collector current	3	A
I_{CM}	Collector current current ($t_p < 5ms$)	7	A
I_B	Base current	1	A
P_{TOT}	Total dissipation at $T_{case} = 25^\circ C$	30	W
T_{stg}	Storage temperature	-65 to 150	$^\circ C$
T_J	Max. operating junction temperature	150	$^\circ C$

2 Electrical characteristics

($T_{case} = 25^{\circ}C$ unless otherwise specified)

Table 3. Electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector cut-off current ($I_E = 0$)	$V_{CB} = 80V$			0.1	mA
I_{EBO}	Emitter cut-off current ($I_C = 0$)	$V_{EB} = 5V$			1	mA
$V_{CEO(sus)}^{(1)}$	Collector-emitter sustaining voltage ($I_B = 0$)	$I_C = 100mA$	80			V
$V_{CE(sat)}^{(1)}$	Collector-emitter saturation voltage	$I_C = 1A$ $I_B = 0.1A$			0.8	V
$V_{BE}^{(1)}$	Base-emitter voltage	$I_C = 1.5A$ $V_{CE} = 2V$			1.3	V
h_{FE}	DC current gain	$I_C = 150mA$ $V_{CE} = 2V$ $I_C = 1A$ $V_{CE} = 2V$	40 15			

Note (1) Pulsed duration = 300 μs , duty cycle $\leq 1.5\%$

2.1 Electrical characteristic (curves)

Figure 2. Safe operating area

Figure 3. Derating curve

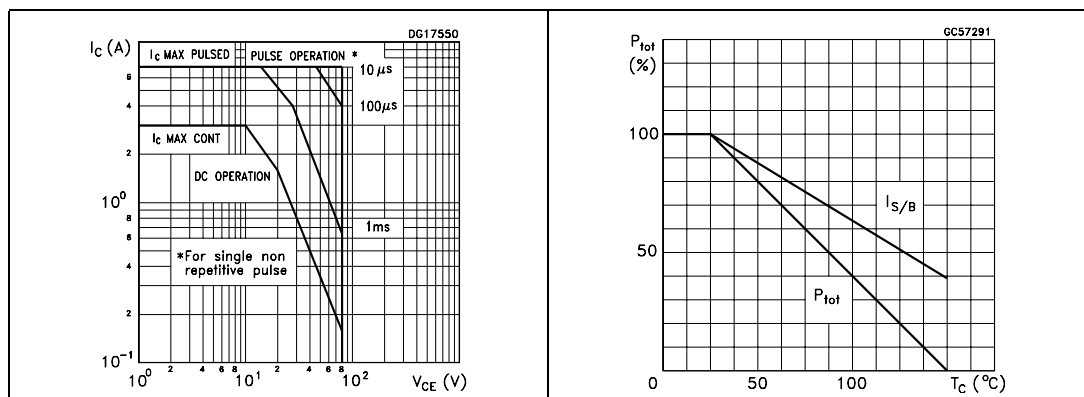


Figure 4. DC current gain

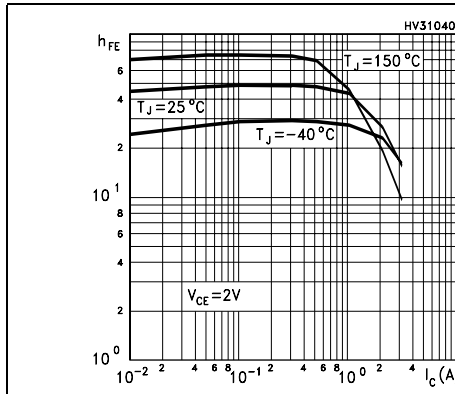


Figure 5. DC current gain

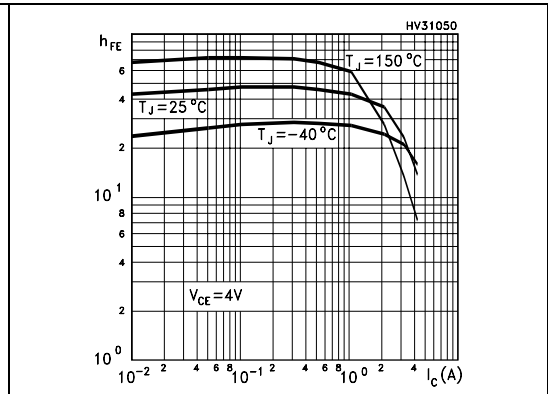


Figure 6. Collector-emitter saturation voltage

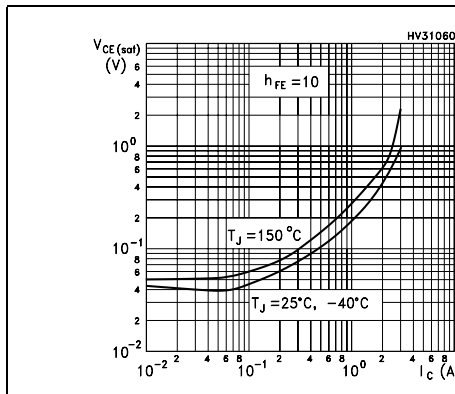


Figure 7. Base-emitter saturation voltage

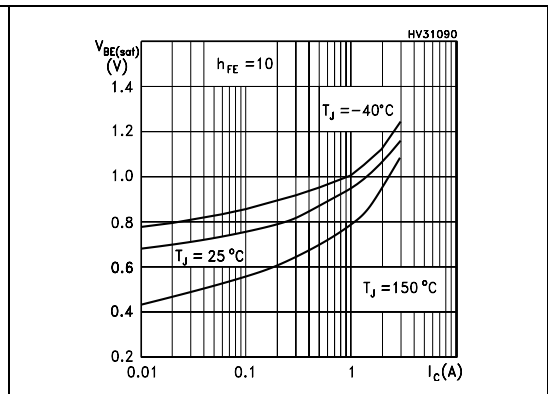


Figure 8. Base-emitter on voltage

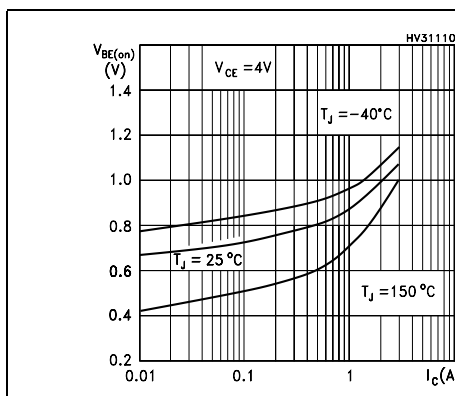


Figure 9. Resistive load switching time

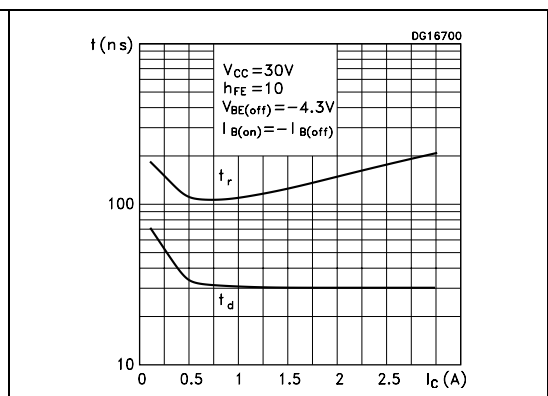
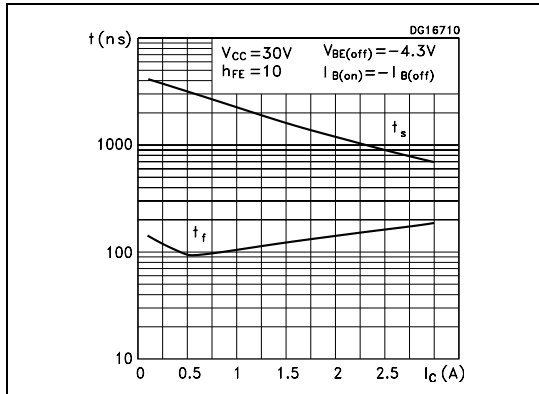
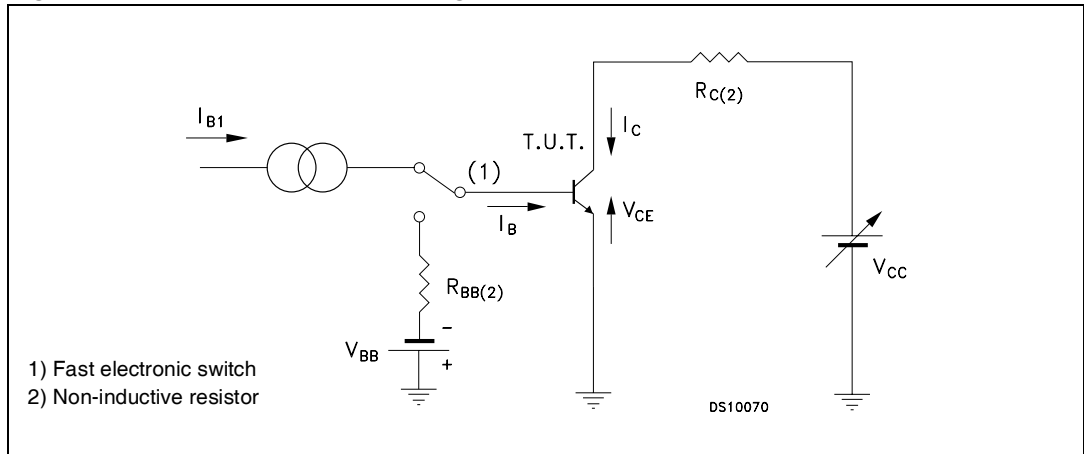


Figure 10. Resistive load switching time



2.2 Test circuits

Figure 11. Resistive load switching test circuit

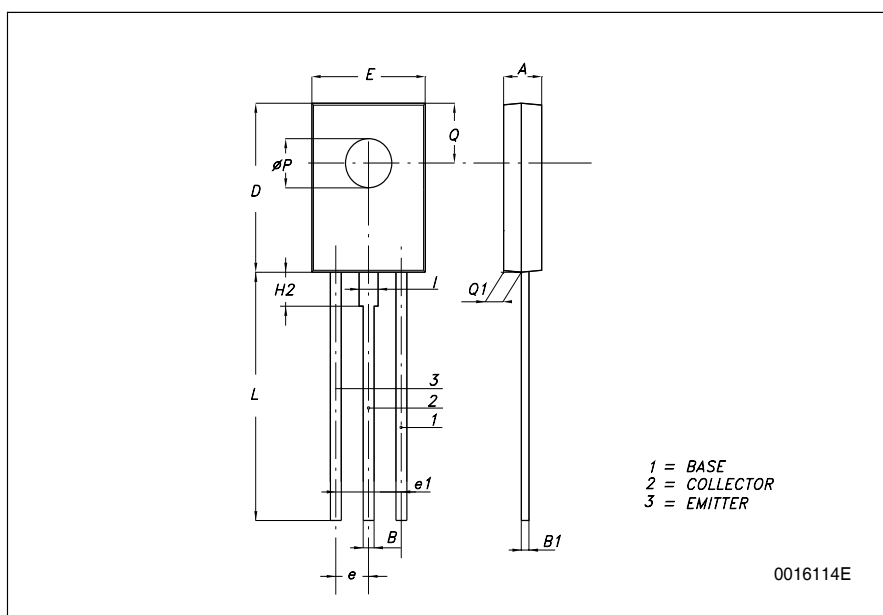


3 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

SOT-32 (TO-126) MECHANICAL DATA

DIM.	mm.		
	MIN.	TYP	MAX.
A	2.4		2.9
B	0.64		0.88
B1	0.39		0.63
D	10.5		11.05
E	7.4		7.8
e	2.04	2.29	2.54
e1	4.07	4.58	5.08
L	15.3		16
P	2.9		3.2
Q		3.8	
Q1	1		1.52
H2		2.15	
l		1.27	



4 Revision history

Table 4. Revision history

Date	Revision	Changes
01-Dec-2000	1	Initial release.
02-Jul-2007	2	Figures 2,3,4,5,6,7, 8, 9 and figure 10 have been added.

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