Table 8: Absolute Maximum Ratings (Die)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pad	(V_{SS} – 0.3V) to (V_{CC} + 0.3V)
Voltage applied to any pad (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
V_{CC} – V_{SS}	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 9: Operating Conditions (Die)

Condition	Value
Commercial operating temperature range	0°C to +50°C
Supply voltage (V_{CC})[1]	+4.5 V to +6.5 V
Ground voltage (V_{SS})[2]	0 V

1. $V_{CC} = V_{CCA} = V_{CCD}$.
2. $V_{SS} = V_{SSA} = V_{SSD}$.

Table 10: DC Parameters (Die)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –1.6 mA
I_{CC}	V_{CC} Current (Operating)		15	30	mA	V_{CC} = 5.5 V [3], R_{EXT} = ∞
I_{SB}	V_{CC} Current (Standby)		0.5	10	µA	[3] [4]
I_{IL}	Input Leakage Current			±1	µA	
I_{ILPD}	Input Current HIGH w/Pull Down			130	µA	Force V_{CC} [5]
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance	4	9	17	KΩ	Pins 17, 18
$R_{ANA\ IN}$	ANA IN Input Resistance	2.5	3	5	KΩ	
A_{PRE1}	Preamp Gain 1	20	23	26	dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		–45	–15	dB	AGC = 2.5 V
A_{ARP}	ANA IN to SP+/– Gain	20	22	25	dB	

Table 10: DC Parameters (Die)

Symbol	Parameters	Min(2)	Typ (1)	Max(2)	Units	Conditions
R_{AGC}	AGC Output Resistance	2.5	5	9.5	KΩ	
I_{PREH}	Preamp Out Source		–2		mA	@ V_{OUT} = 1.0 V
I_{PREL}	Preamp In Sink		0.5		mA	@ V_{OUT} = 2.0 V

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} connected together.*
4. *$\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$ must be at V_{CCD} .*
5. *XCLK pin.*

Table 11: AC Parameters (Die)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
F_S	Sampling Frequency	ISD1416 ISD1420			8 6.4	KHz KHz	(5) (5)
F_{CF}	Filter Pass Band	ISD1416 ISD1420		3.3 2.6		KHz KHz	3 dB Roll-Off Point (3)(6) 3 dB Roll-Off Point (3)(6)
T_{REC}	Record Duration	ISD1416 ISD1420	16 20			sec sec	
T_{PLAY}	Playback Duration	ISD1416 ISD1420	16 20			sec sec	(5) (5)
T_{LED1}	$\overline{RECLED}$ ON Delay			5		msec	
T_{LED2}	$\overline{RECLED}$ OFF Delay	ISD1416 ISD1420	30 40	38.9 48.6	95 110	msec msec	
T_{SET}	Address Setup Time		300			nsec	
T_{HOLD}	Address Hold Time		0			nsec	
T_{RPUD}	Record Power-Up Delay	ISD1416 ISD1420		26 32		msec msec	
T_{RPDD}	Record Power-Down Delay	ISD1416 ISD1420		26 32		msec msec	
T_{PPUD}	Play Power-Up Delay	ISD1416 ISD1420		26 32		msec msec	

Table 11: AC Parameters (Die)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
T_{PPDD}	Play Power-Down Delay	ISD1416 ISD1420		6.5 8.1		msec msec	
T_{EOM}	EOM Pulse Width	ISD1416 ISD1420		12.5 15.625		msec msec	
THD	Total Harmonic Distortion			1	3	%	@ 1 KHz
P_{OUT}	Speaker Output Power			12.2		mW	R_{EXT} = 16 Ω
V_{OUT}	Voltage Across Speaker Pins			1.25	2.5	V p–p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage				20	mV	Peak-to-Peak (4)
V_{IN2}	ANA IN Input Voltage				50	mV	Peak-to-Peak

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).*
4. *With 5.1 KΩ series resistor at ANA IN.*
5. *Sampling frequency and playback duration will vary as much as ±2.25 percent over the commercial temperature and voltage ranges. All devices will meet the maximum sampling frequency and minimum playback duration parameters. For greater stability, an external clock can be utilized (see Pin Descriptions).*
6. *Filter specification applies to the antialiasing filter and to the smoothing filter.Typical Parameter Variation with Voltage and Temperature (Die).*

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (DIE)

Chart 5: Record Mode Operating Current (I_{CC})

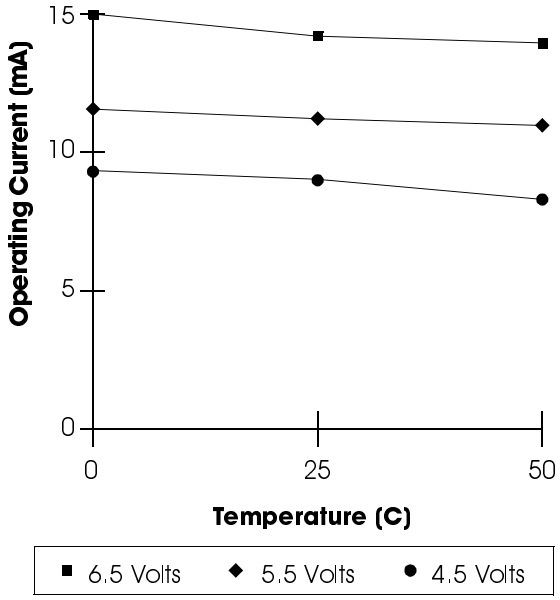


Chart 6: Total Harmonic Distortion

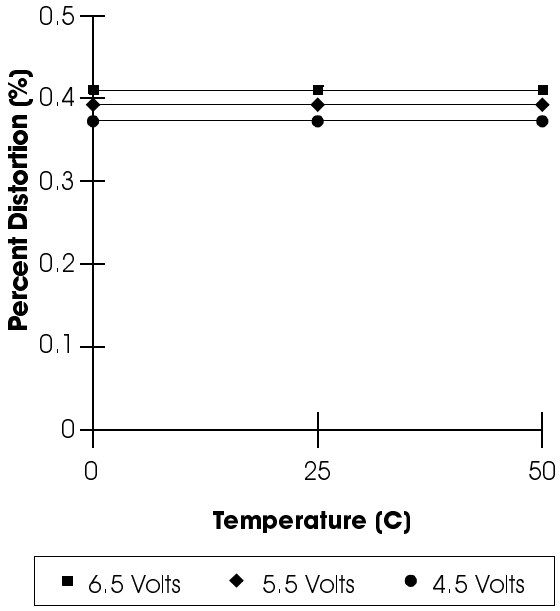


Chart 7: Standby Current (I_{SB})

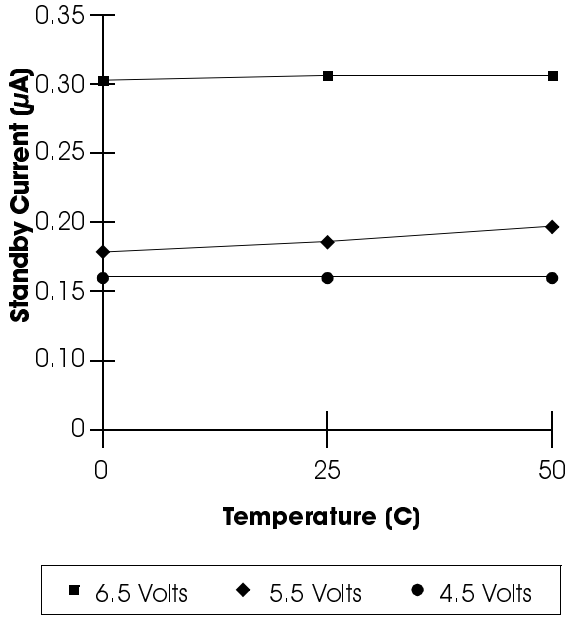


Chart 8: Oscillator Stability

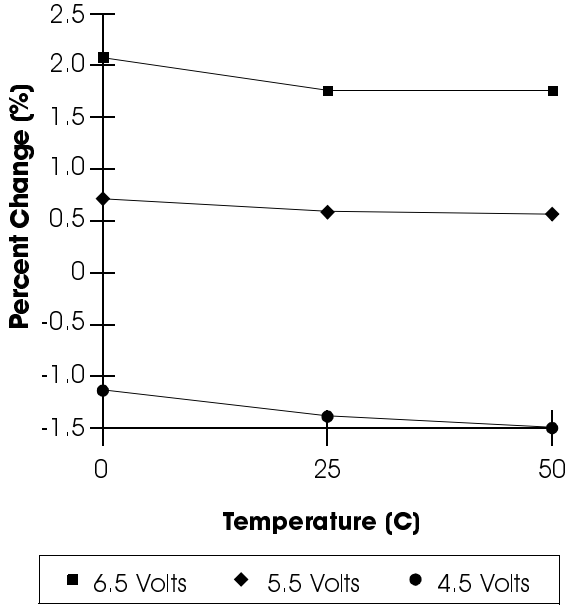
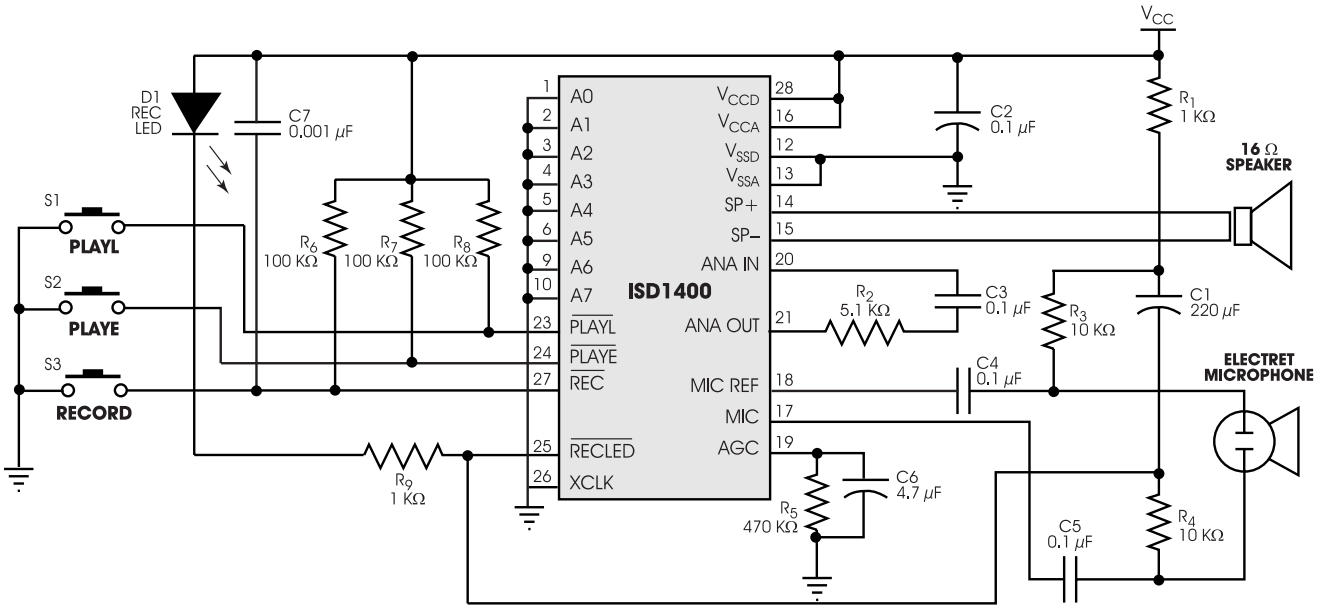


Figure 4: Application Example



FUNCTIONAL DESCRIPTION EXAMPLE

The following example operating sequence demonstrates the functionality of the ISD1400 series devices.

1. Record a message filling the address space.

   Pulling the $\overline{\text{REC}}$ signal LOW initiates a record cycle from the beginning of the message space. If $\overline{\text{REC}}$ is held LOW, the recording continues until the message space has been filled. Once the message space is filled, recording ceases. The device will automatically power down after $\overline{\text{REC}}$ is pulled HIGH.

2. Edge-activated playback.

   Pulling the $\overline{\text{PLAYE}}$ signal LOW initiates a playback cycle from the beginning of the message space or at a selected location. The rising edge of $\overline{\text{PLAYE}}$ has no effect on operation. If a recording has filled the message space, the entire message is played. When the device reaches the EOM marker, it automatically powers down. A subsequent falling edge on $\overline{\text{PLAYE}}$ initiates a new play cycle from the start address.

3. Level-activated playback.

   Pulling the $\overline{\text{PLAYL}}$ signal LOW initiates a playback cycle from the beginning of the message space or a selected location. If recording has filled the message space, the entire message is played. When the device reaches the EOM marker, it automatically powers down. A subsequent falling edge on $\overline{\text{PLAYL}}$ initiates a new play cycle from the starting address.

4. Level-activated playback (truncated).

   If $\overline{\text{PLAYL}}$ is pulled HIGH any time during the playback cycle, the device stops playing and enters the power-down mode. A subsequent falling edge on $\overline{\text{PLAYL}}$ initiates a new play cycle from the start address.

5. Record (interrupting playback).

   The $\overline{\text{REC}}$ signal takes precedence over other operations. Any LOW-going transition

on $\overline{REC}$ initiates a new record operation from the beginning of the start address or at a selected location, regardless of any current operation in progress.

6. Record a message, partially filling the address space.

   A record operation need not fill the entire message space. Releasing the $\overline{REC}$ signal HIGH before filling the message space causes the recording to stop and an EOM to be placed. The device powers down automatically.

7. Play back a message, partially filling the address space.

   Pulling the $\overline{PLAYE}$ or $\overline{PLAYL}$ signal LOW initiates a playback cycle which is then completed when the EOM marker is encountered. Playback ceases and the device powers down.

8. $\overline{RECLED}$ operation.

   The $\overline{RECLED}$ output pin provides an active-LOW signal which can be used to drive an LED as a "record-in-progress" indicator. It returns to a HIGH state when the $\overline{REC}$ pin is released HIGH or when the recording is completed due to the message space being filled. This pin also pulses LOW to indicate an EOM at the end of a message being played.

APPLICATIONS NOTE

Some users may experience an unexpected recording taking place when their circuit is powered up, or the batteries are changed and V_{CC} rises faster than $\overline{REC}$. This undesired recording prevents playback of the previously recorded message. A spurious End Of Message (EOM) marker appears at the very beginning of the memory, preventing access to the original message, and nothing is played.

To prevent this occurrence, place a capacitor (approx. 0.001 μF) between the control pin ($\overline{REC}$) and V_{CC}. This pulls the control pin voltage up with V_{CC} as it rises. Once the voltage is HIGH, the pull-up device will keep the pin HIGH until intentionally pulled LOW, preventing the false EOM marker.

Since this anomaly depends on factors such as the capacitance of the user's printed circuit board, not all circuit designs will exhibit the spurious marker. However, it is recommended that the capacitor is included for design reliability. A more detailed explanation and resolution of this occurrence is described in Application Information.

ISD1400 SERIES PHYSICAL DIMENSIONS

Figure 5: 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP) (P)

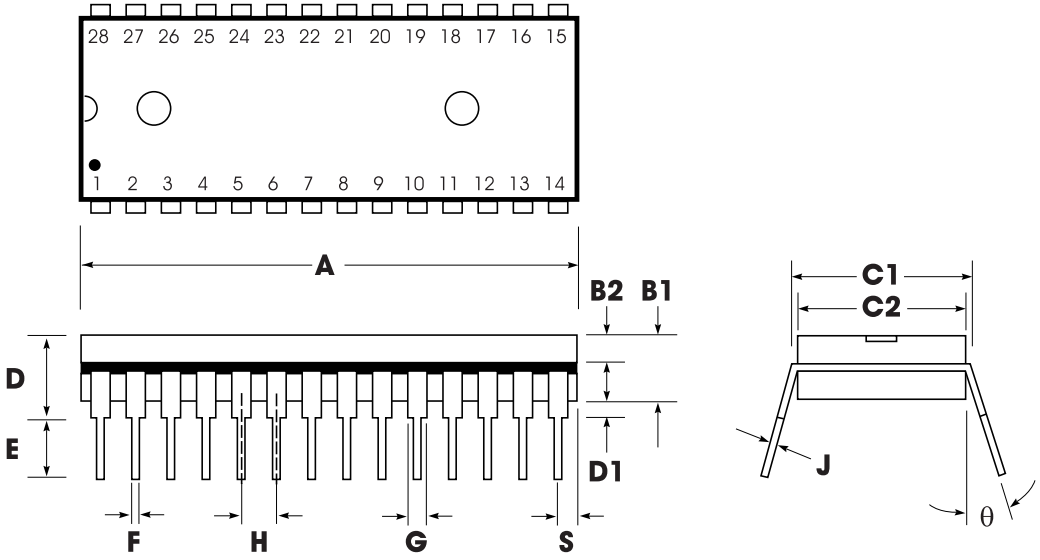


Table 12: Plastic Dual Inline Package (PDIP) (P) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.65
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
q	0°		15°	0°		15°

NOTE: *Lead coplanarity to be within 0.005 inches.*

Figure 6: 28-Lead 0.300-Inch Plastic Small Outline Integrated Circuit (SOIC) (S)

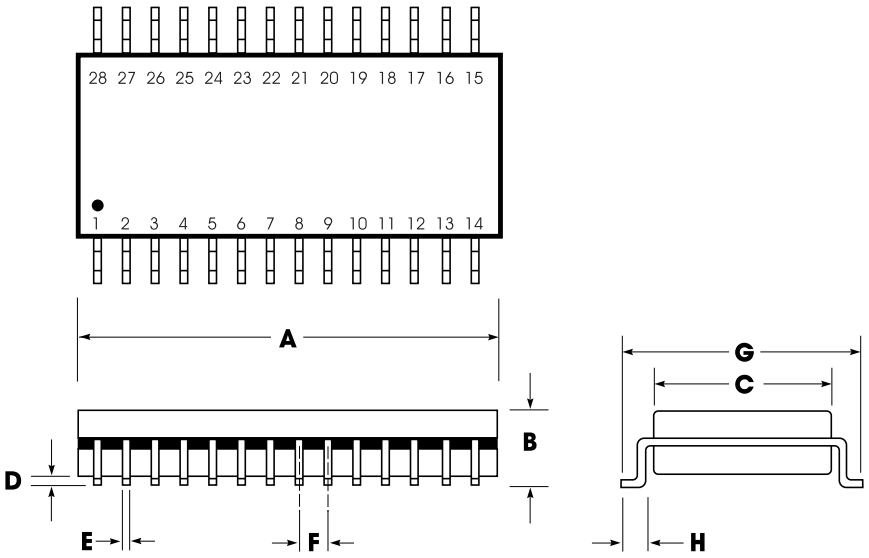


Table 13: Plastic Small Outline Integrated Circuit (SOIC) (S) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.019	0.35	0.41	0.48
F		0.050			1.27	
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

NOTE: *Lead coplanarity to be within 0.004 inches.*

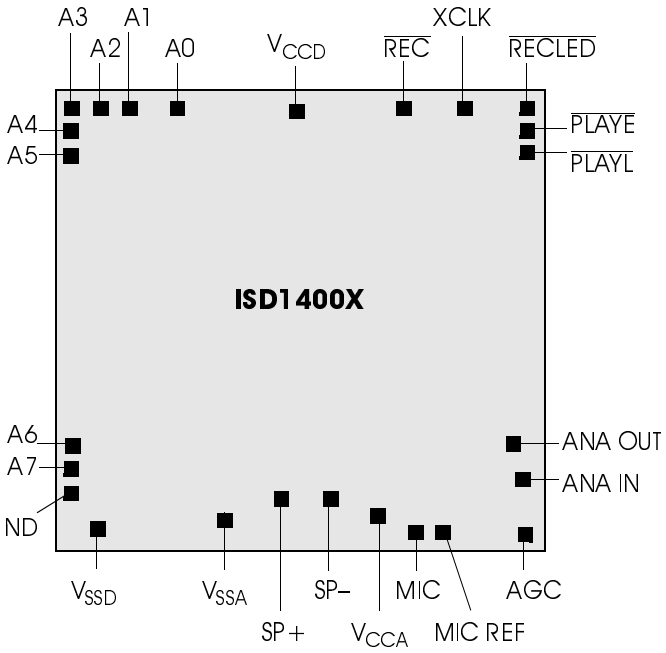
Figure 7: ISD1400 Series Bonding Physical Layout[1]

ISD1400X

I. Die Dimensions
X: 172.2 ±1 mils
Y: 168.5 ±1 mils

II. Die Thickness[(2)]
17.5 ±1 mils

III. Pad Opening
100 x 112 microns
3.9 x 4.4 mils



1. *The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.*
2. *Die thickness is subject to change, please contact ISD factory for status.*

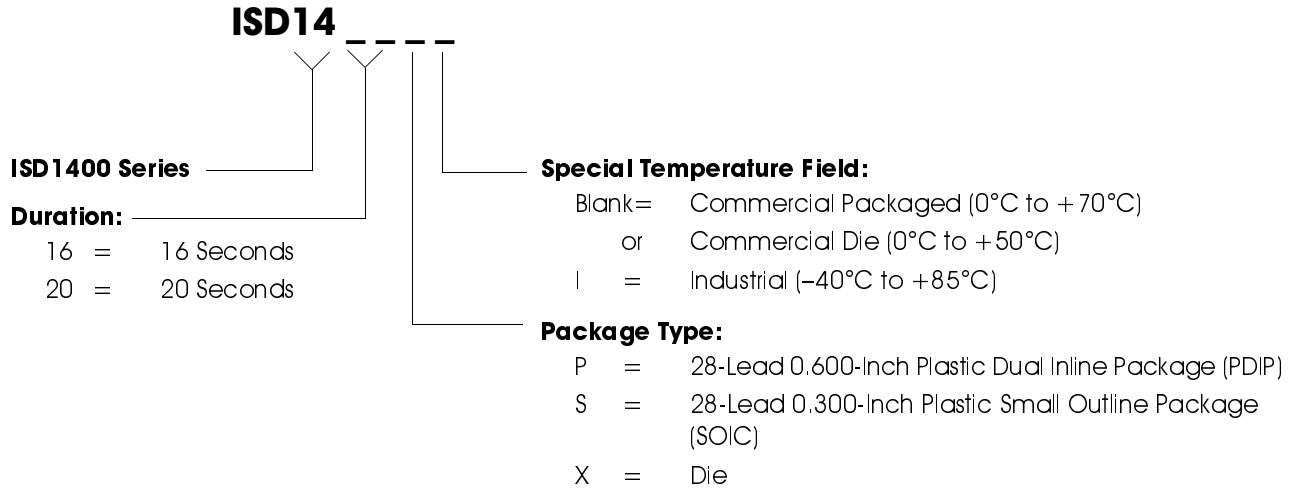
Table 14: ISD1400 Series PIN/PAD Designations, with Respect to Die Center (µm)

Pin	Pin Name	X Axis	Y Axis
A0	Address 0	–1332.5	1973.8
A1	Address 1	–1628.9	1973.8
A2	Address 2	–1808.9	1973.8
A3	Address 3	–2014.1	1910.2
A4	Address 4	–2014.1	1722.6
A5	Address 5	–2014.1	1519.8
A6	Address 6	–2014.1	–1214.6
A7	Address 7	–2014.1	–1399.8
NC	No Connect	–2014.1	–1745.4
V_{SSD}	V_{SS} Digital Power Supply	–1894.1	–1971.8
V_{SSA}	V_{SS} Analog Power Supply	–358.1	–1971.8
SP+	Speaker Output +	–17.7	–1896.6
SP–	Speaker Output –	411.9	–1896.6
V_{CCA}	V_{CC} Analog Power Supply	779.5	–1936.2
MIC	Microphone Input	991.5	–1973.8
MIC REF	Microphone Reference	1168.7	–1973.8
AGC	Automatic Gain Control	1977.9	–1910.6
ANA IN	Analog Input	2005.1	–1580.2
ANA OUT	Analog Output	1990.7	–1379.0
$\overline{\text{PLAYL}}$	Level-Activated Playback	2013.9	1608.6
$\overline{\text{PLAYE}}$	Edge-Activated Playback	2013.9	1777.0
$\overline{\text{RECLED}}$	Record LED Output	2011.9	1971.8
XCLK	No Connect (optional)	1580.7	1973.8
$\overline{\text{REC}}$	Record	752.3	1973.8
V_{CCD}	V_{CC} Digital Power Supply	–48.5	1929.4

NOTE: *Die dimensions and pin/pad positions may be subject to change. Please contact ISD Sales Offices or Representatives to verify current or future specifications.*

ORDERING INFORMATION

Product Number Descriptor Key



When ordering ISD1400 Series devices, please refer to the following valid part numbers.

Part Number	Part Number
ISD1416P	ISD1420P
ISD1416PI	ISD1420PI
ISD1416S	ISD1420S
ISD1416SI	ISD1420SI
ISD1416X	ISD1420X

For the latest product information, access ISD's worldwide website at http://www.isd.com.