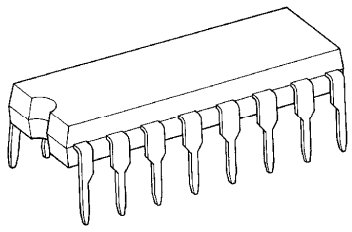
TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TD62308AP, TD62308F, TD62308AF

4CH LOW INPUT ACTIVE HIGH-CURRENT DARLINGTON SINK DRIVER

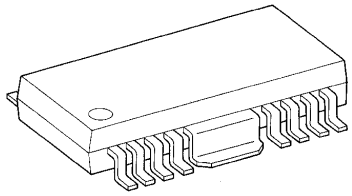
The TD62308AP / F / AF are non-inverting transistor array which are comprised of four NPN darlington output stages and PNP input stages.
These devices are low level input active driver and are suitable for operation with TTL, 5V CMOS and 5V Microprocessor which have sink current output drivers. Applications include relay, hammer, lamp and stepping moter drivers.

TD62308AP



DIP16-P-300-2.54A

TD62308F
TD62308AF



HSOP16-P-300-1.00

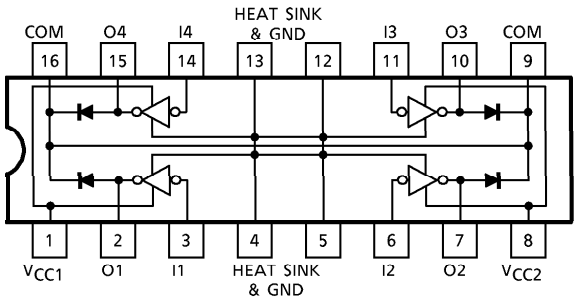
FEATURES

- Output current (single output) 1.5A (Max.)
- High sustaining voltage output 35V (Min.) (TD62308F)
  50V (Min.)
  (TD62308AP, TD62308AF)
- Output clamp diodes
- Input compatible with TTL and 5V CMOS
- Low level active inputs
- Standard supply voltage
- Two V_{CC} terminals V_{CC1}, V_{CC2} (separeted)
- GND and SUB terminal = heat sink
- Package type-AP : DIP-16pin
- Package type-F, AF : PFP-16pin

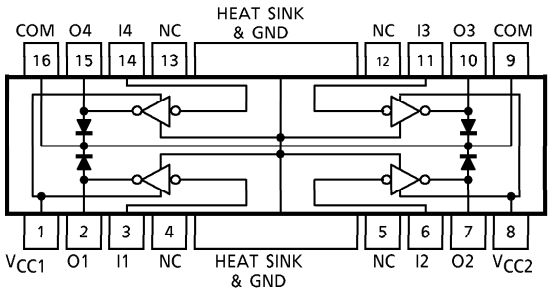
Weight
DIP16-P-300-2.54A : 1.11g (Typ.)
HSOP16-P-300-1.00 : 0.50g (Typ.)

PIN CONNECTION (TOP VIEW)

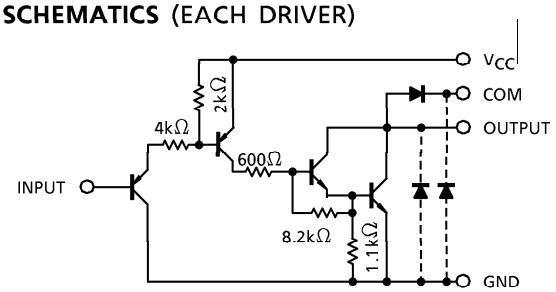
TD62308AP



TD62308F, TD62308AF



SCHEMATICS (EACH DRIVER)



(Note) The input and output parasitic diodes cannot be used as clamp diodes.

961001EBA2

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}	−0.5~10	V
Output Sustaining Voltage	F	$V_{CE\ (SUS)}$	−0.5~35	V
	AP, AF		−0.5~50	
Output Current		I_{OUT}	1.5	A / ch
Input Current		I_{IN}	−10	mA
Input Voltage		V_{IN}	−0.5~30	V
Clamp Diode Reverse Voltage	F	V_R	35	V
	AP, AF		50	
Clamp Diode Forward Current		I_F	1.5	A
Power Dissipation	AP	P_D	1.47 / 2.7 (Note 1)	W
	F, AF		0.9 / 1.4 (Note 2)	
Operating Temperature		T_{opr}	−40~85	°C
Storage Temperature		T_{stg}	−55~150	°C

(Note 1) On Glass Epoxy (50 × 50 × 1.6mm Cu 50%)
(Note 2) On Glass Epoxy (60 × 30 × 1.6mm Cu 30%)

RECOMMENDED OPERATING CONDITIONS (Ta = −40~85°C)

CHARACTERISTIC		SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT
Supply Voltage		V_{CC}	—		4.5	—	5.5	V
Output Sustaining Voltage	F	$V_{CE\ (SUS)}$	—		0	—	35	V
	AP, AF		—		0	—	50	
Output Current	AP	I_{OUT}	DC 1 circuit, Ta = 25°C		0	—	1250	mA / ch
			T_{pw} = 25ms, 4 circuits, Ta = 85°C, T_j = 120°C	Duty = 10%	0	—	1250	
				Duty = 50%	0	—	700	
	F, AF			Duty = 10%	0	—	1250	
				Duty = 50%	0	—	390	
Input Voltage		V_{IN}	—		0	—	25	V
Input Voltage	Output On	$V_{IN\ (ON)}$	—		0	—	V_{CC} − 3.6	V
	Output Off	$V_{IN\ (OFF)}$	—		V_{CC} − 1.0	—	V_{CC}	
Clamp Diode Reverse Voltage	F	V_R	—		—	—	35	V
	AP, AF		—		—	—	50	
Clamp Diode Forward Current		I_F	—		—	—	1.25	A
Power Dissipation	AP	P_D	Ta = 85°C (Note 1)		—	—	1.4	W
	F, AF		Ta = 85°C (Note 2)		—	—	0.7	

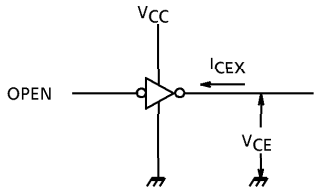
(Note 1) On Glass Epoxy (50 × 50 × 1.6mm Cu 50%)
(Note 2) On Glass Epoxy (60 × 30 × 1.6mm Cu 30%)

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

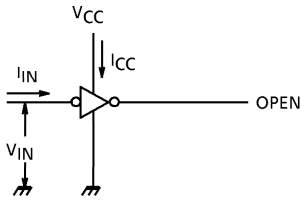
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Leakage Current	AP, AF	I_{CEX}	1	V_{CE} = 50V, Ta = 25°C		—	—	50	μA
				V_{CE} = 50V, Ta = 85°C		—	—	100	
	F			V_{CE} = 35V, Ta = 25°C		—	—	50	
				V_{CE} = 35V, Ta = 85°C		—	—	100	
Output Saturation Voltage		$V_{CE\ (sat)}$	3	I_{OUT} = 1.25A		—	—	1.8	V
				I_{OUT} = 0.7A		—	—	1.3	
Input Voltage	"H" Level	V_{IH}	—	—		V_{CC} – 1.6	—	25	V
	"L" Level	V_{IL}	—	—		—	—	V_{CC} – 3.6	
Input Current	"H" Level	I_{IH}	—	—		—	—	10	μA
	"L" Level	I_{IL}				—	– 0.05	– 0.36	mA
Clamp Diode Reverse Current	AP, AF	I_R	4	V_R = 50V, Ta = 25°C		—	—	50	μA
	F			V_R = 35V, Ta = 25°C		—	—	50	
Clamp Diode Forward Voltage		V_F	5	I_F = 1.25A		—	1.5	2.0	V
Supply Current	Output On	$I_{CC\ (ON)}$	2	V_{CC} = 5.5V, V_{IN} = 0V		—	8.5	12.5	mA / ch
	Output Off	$I_{CC\ (OFF)}$		V_{CC} = 5.5V, V_{IN} = V_{CC}		—	—	1.0	μA
Turn-On Delay	F	t_{ON}	6	C_L = 15pF	V_{OUT} = 35V, R_L = 28Ω	—	0.2	—	μs
	AP, AF				V_{OUT} = 50V, R_L = 40Ω				
Turn-Off Delay	F	t_{OFF}			V_{OUT} = 35V, R_L = 28Ω	—	5.0	—	
	AP, AF				V_{OUT} = 35V, R_L = 40Ω				

TEST CIRCUIT

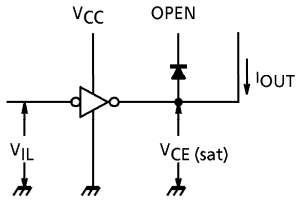
1. I_{CEX}



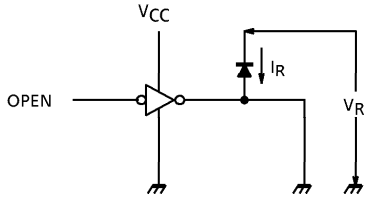
2. I_{CC}



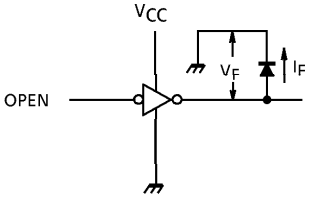
3. $V_{CE\ (sat)}$



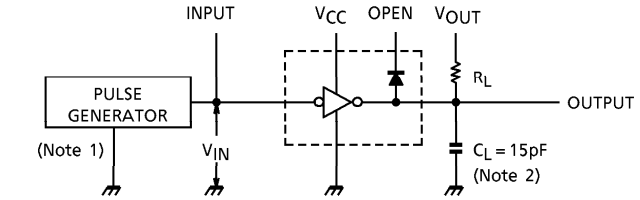
4. I_R

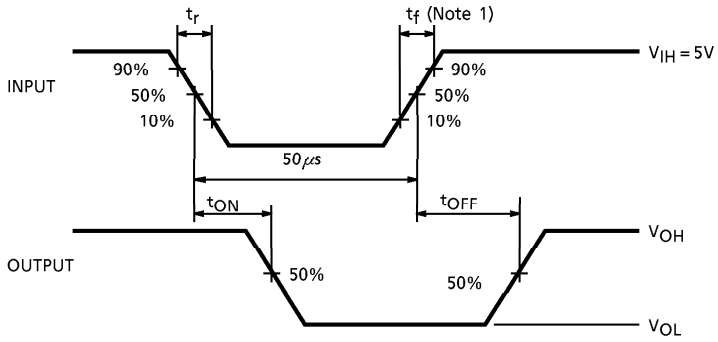


5. V_F



6. t_{ON}, t_{OFF}





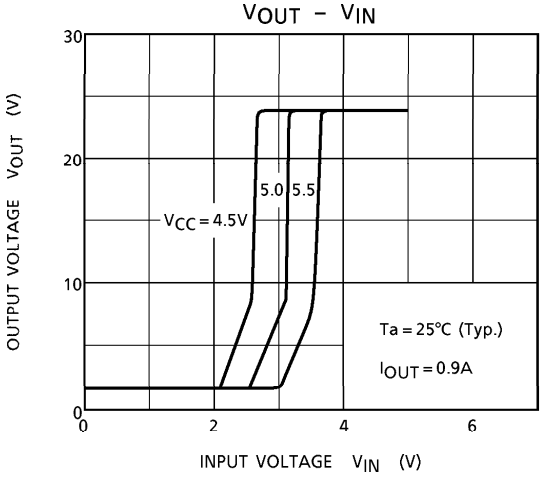
(Note 1) Pulse width 50μs, duty cycle 10%
Output impedance 50Ω $t_r \leqq 5$ns, $t_f \leqq 10$ns

(Note 2) C_L includes probe and jig capacitance.

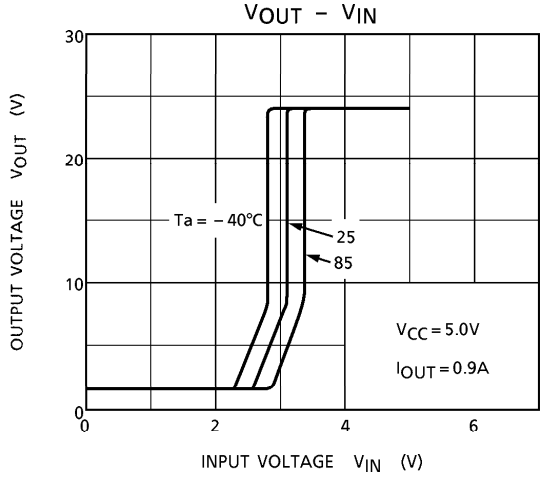
PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, V_{CC}, COMMON and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

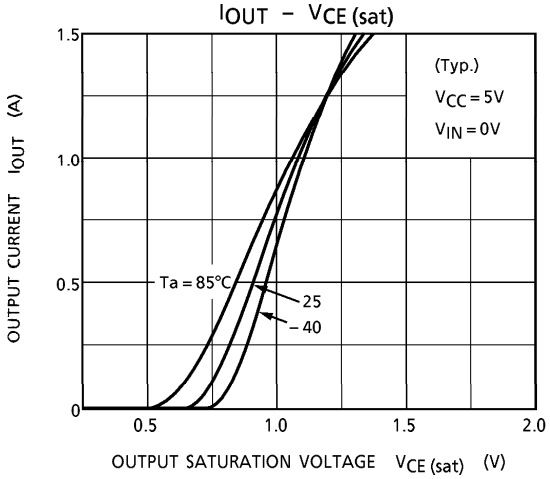
V_{OUT} – V_{IN}



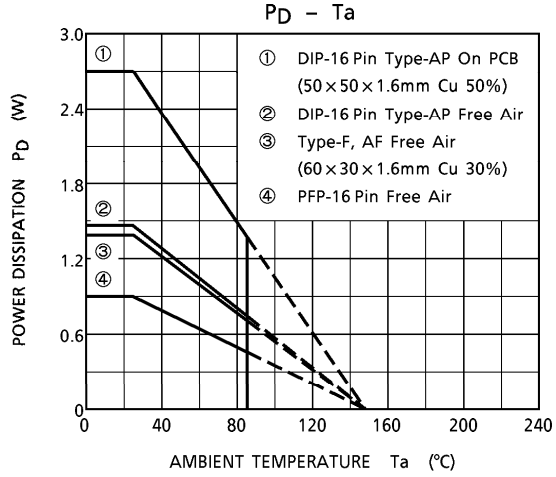
V_{OUT} – V_{IN}



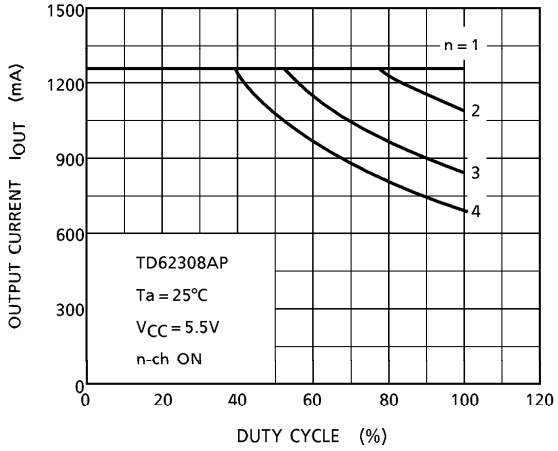
I_{OUT} – $V_{CE\ (sat)}$



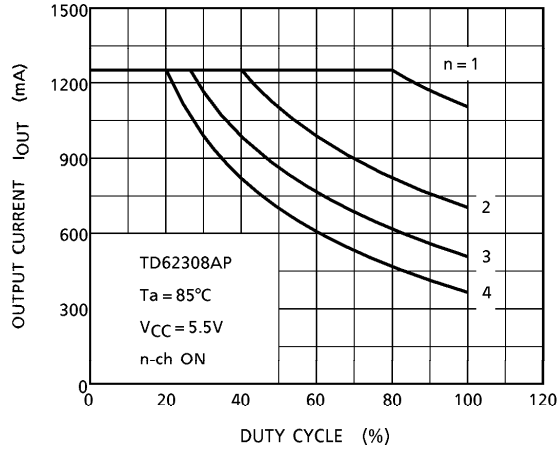
P_D – Ta

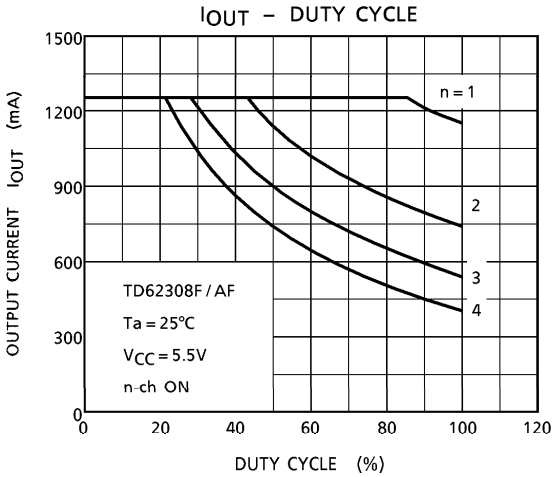


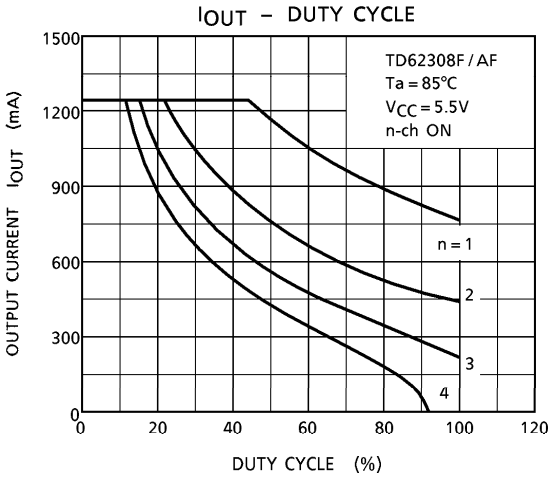
I_{OUT} – DUTY CYCLE



I_{OUT} – DUTY CYCLE



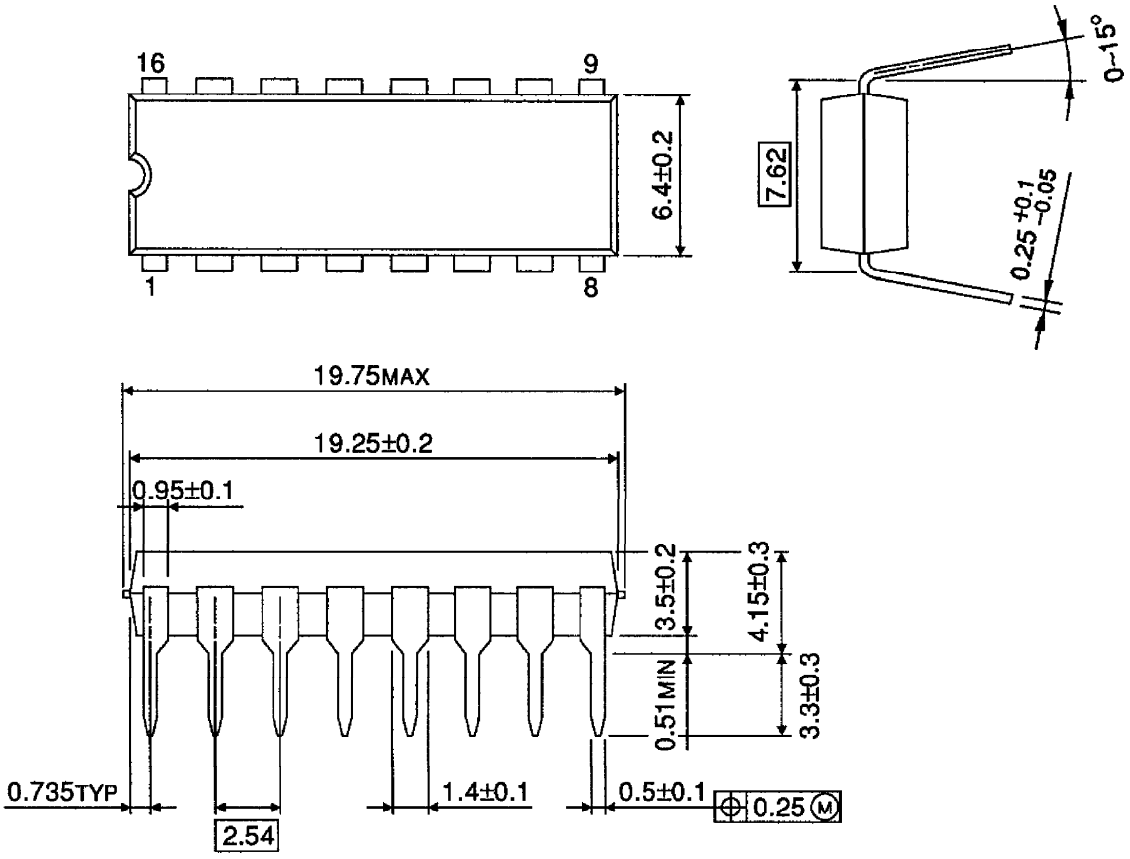

IOUT – DUTY CYCLE
OUTPUT CURRENT IOUT (mA)
1500
1200
900
600
300
0
0
20
40
60
80
100
120
DUTY CYCLE (%)
n = 1
2
3
4
TD62308F / AF
Ta = 25°C
VCC = 5.5V
n-ch ON


IOUT – DUTY CYCLE
OUTPUT CURRENT IOUT (mA)
1500
1200
900
600
300
0
0
20
40
60
80
100
120
DUTY CYCLE (%)
TD62308F / AF
Ta = 85°C
VCC = 5.5V
n-ch ON
n = 1
2
3
4

OUTLINE DRAWING

DIP16-P-300-2.54A

Unit : mm

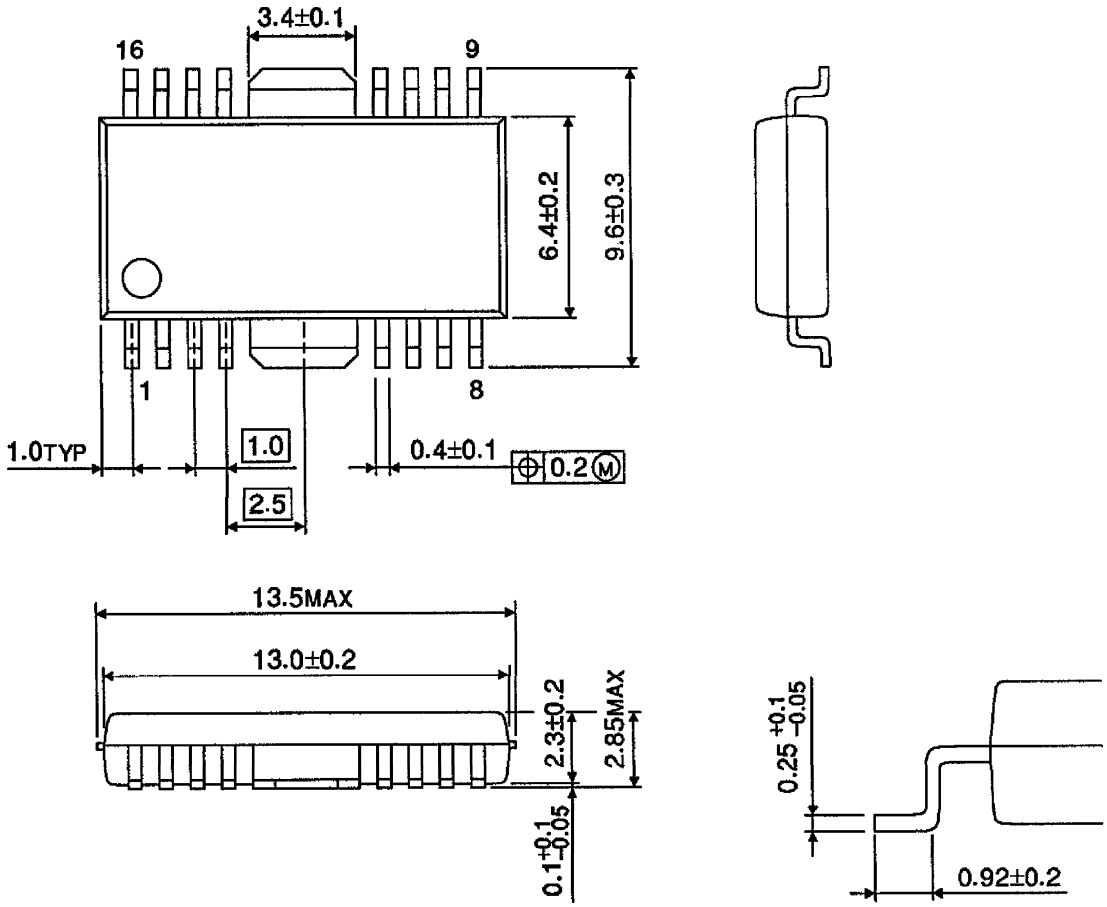


Weight : 1.11g (Typ.)

OUTLINE DRAWING

HSOP16-P-300-1.00

Unit : mm



Weight : 0.50g (Typ.)