

DATA SHEET

TDA1561Q

**2 × 23 W high efficiency car radio
power amplifier**

Preliminary specification
Supersedes data of 1997 Jun 11
File under Integrated Circuits, IC01

1997 Aug 14

2 × 23 W high efficiency car radio power amplifier

TDA1561Q

FEATURES

- Low dissipation due to switching from Single-Ended (SE) to Bridge-Tied Load (BTL) mode
- High Common Mode Rejection Ratio (CMRR)
- Mute/standby/operating/SE-only (mode select pin)
- Zero crossing mute and standby circuit
- Load dump protection circuit
- Short-circuit safe to ground, to supply voltage and across load
- Loudspeaker protection circuit
- Device switches to single-ended operation at excessive junction temperatures.

GENERAL DESCRIPTION

The TDA1561Q is a monolithic power amplifier in a 13 lead single-in-line (SIL) plastic power package. It contains two identical 23 W amplifiers. The dissipation is minimized by switching from SE to BTL mode, only when a higher output voltage swing is needed. The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _P	supply voltage	DC biased	6.0	14.4	18	V
		non operating	–	–	30	V
		load dump	–	–	50	V
I _{ORM}	repetitive peak output current		–	–	4	A
I _{q(tot)}	total quiescent current	R _L = ∞	–	95	150	mA
I _{stb}	standby current		–	1	50	μA
Z _i	input impedance		–	60	–	kΩ
P _o	output power	RL = 4 Ω; EIAJ	–	36	–	W
		THD 10%	21	23	–	W
G _v	voltage gain		31	32	33	dB
CMRR	common mode rejection ratio	f = 1 kHz; R _s = 0 Ω	–	80	–	dB
SVRR	supply voltage ripple rejection	f = 1 kHz; R _s = 0 Ω	45	55	–	dB
ΔV _O	DC output offset voltage		–	–	150	mV
α _{cs}	channel separation	R _s = 0 kΩ	40	60	–	dB
ΔG _v	channel unbalance		–	–	1	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1561Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

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BLOCK DIAGRAM

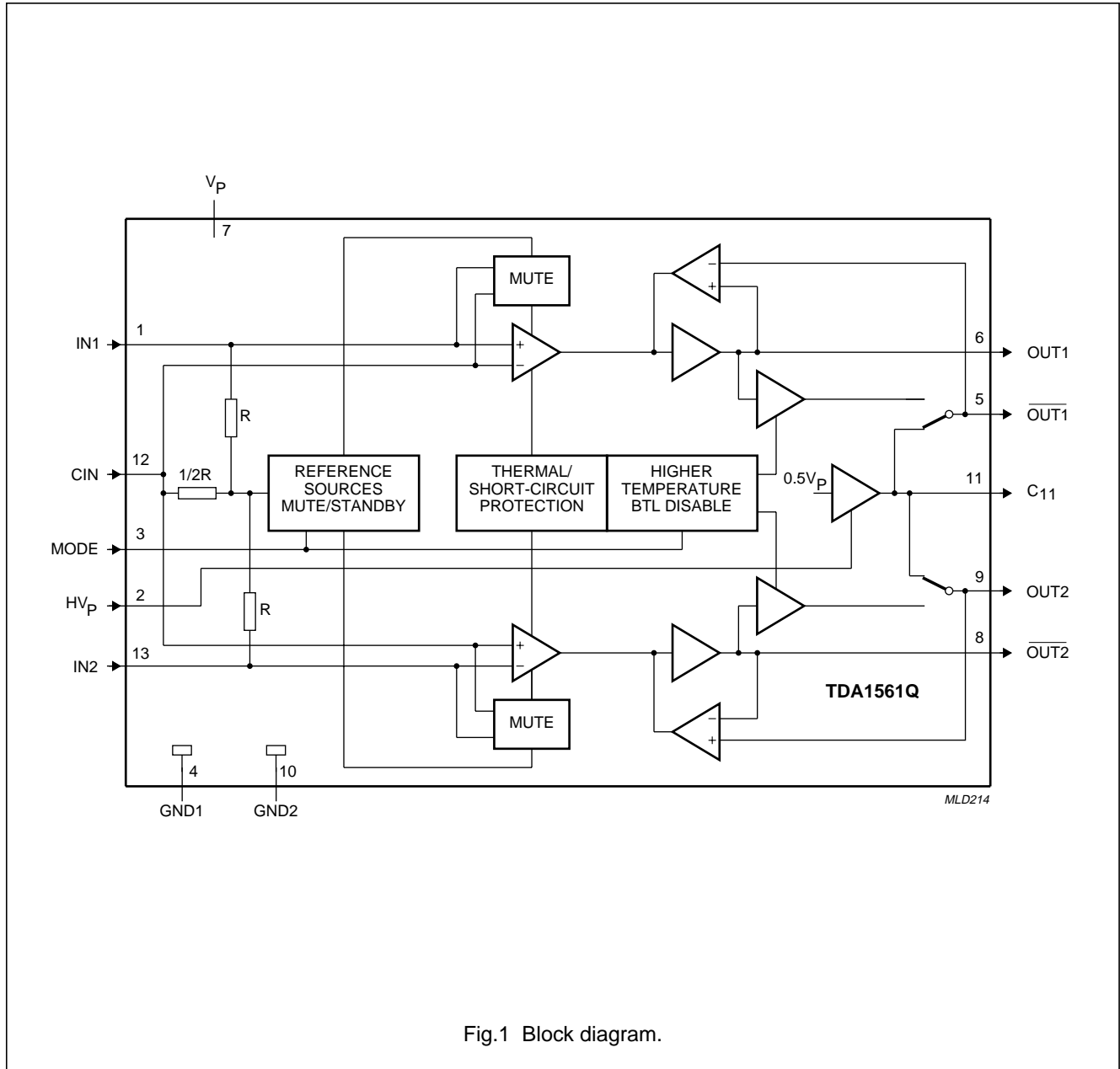


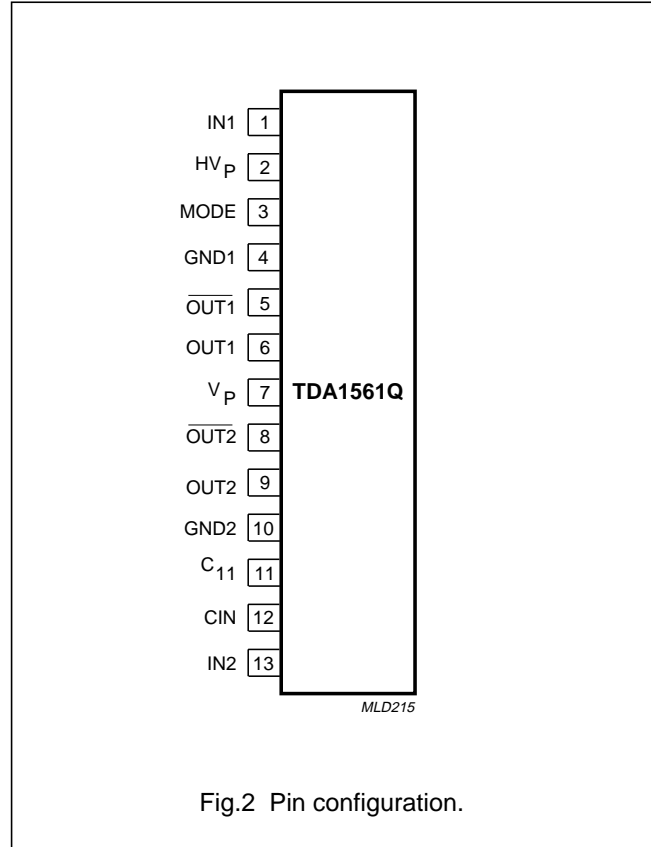
Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
IN1	1	input 1
HV _P	2	half supply voltage control input
MODE	3	mute/standby/operating/SE-only
GND1	4	ground 1
$\overline{\text{OUT1}}$	5	inverting output 1
OUT1	6	non-inverting output 1
V _P	7	supply voltage
$\overline{\text{OUT2}}$	8	inverting output 2
OUT2	9	non-inverting output 2
GND2	10	ground 2
C ₁₁	11	electrolytic capacitor for single-ended (SE) mode
CIN	12	common input
IN2	13	input 2



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FUNCTIONAL DESCRIPTION

The TDA1561Q contains two identical amplifiers with differential inputs. At low output power (up to output amplitudes of 3 V (RMS) at $V_P = 14.4$ V), the device operates as a normal SE amplifier. When a larger output voltage swing is needed, the circuit switches internally to BTL operation.

With a sine wave input signal the dissipation of a conventional BTL amplifier up to 2 W output power is more than twice the dissipation of the TDA1561Q (see Fig.9).

In normal use, when the amplifier is driven with music-like signals, the high (BTL) output power is only needed for a small percentage of time. Under the assumption that a music signal has a normal (Gaussian) amplitude distribution, the dissipation of a conventional BTL amplifier with the same output power is approximately 70% higher (see Fig.10).

The heatsink has to be designed for use with music signals. With such a heatsink, the thermal protection will disable the BTL mode when the junction temperature exceeds 145 °C. In this case the output power is limited to 5 W per amplifier.

The gain of each amplifier is internally fixed at 32 dB. With the MODE pin, the device can be switched to the following modes:

- Standby with low standby current (<50 μ A)
- Mute condition, DC adjusted
- On, operation
- SE-only, operation (BTL disabled).

The device is fully protected against short-circuiting of the output pins to ground and to the supply voltage. It is also protected against short-circuiting the loudspeaker and high junction temperatures. In the event of a permanent short-circuit condition to ground or the supply voltage, the output stage will be switched off causing a low dissipation. With permanent short-circuiting of the loudspeaker, the output stage will be repeatedly switched on and off. The duty cycle in the 'on' condition is low enough to prevent excessive dissipation.

To avoid pops during switching from 'mute' to 'on' or from 'on' to 'mute/standby' while an input signal is present, a built-in zero-crossing detector allows only switching at zero input voltage. However, when the supply voltage drops below 6 V (e.g. engine start), the circuit mutes immediately avoiding clicks coming from electronic circuitry preceding the power amplifier.

The voltage of the SE electrolytic capacitor (pin 11) is always kept at $0.5V_P$ by means of a voltage buffer (see Fig.1). The value of this capacitor has an important influence on the output power in SE mode, especially at low signal frequencies, a high value is recommended to minimize dissipation at low frequencies.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _P	supply voltage	operating	–	18	V
		non operating	–	30	V
		load dump; t _r > 2.5 ms	–	50	V
V _{P(sc)}	short-circuit safe voltage		–	18	V
V _{rp}	reverse polarity voltage		–	6	V
I _{OSM}	non-repetitive peak output current		–	6	A
I _{ORM}	repetitive peak output current		–	4	A
P _{tot}	total power dissipation		–	60	W
T _{stg}	storage temperature		–55	+150	°C
T _{vj}	virtual junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–40	–	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-c)}	thermal resistance from junction to case	see note 1	1.3	K/W
R _{th(j-a)}	thermal resistance from junction to ambient		40	K/W

Note

1. The value of R_{th(c-h)} depends on the application (see Fig.3).

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Heatsink design

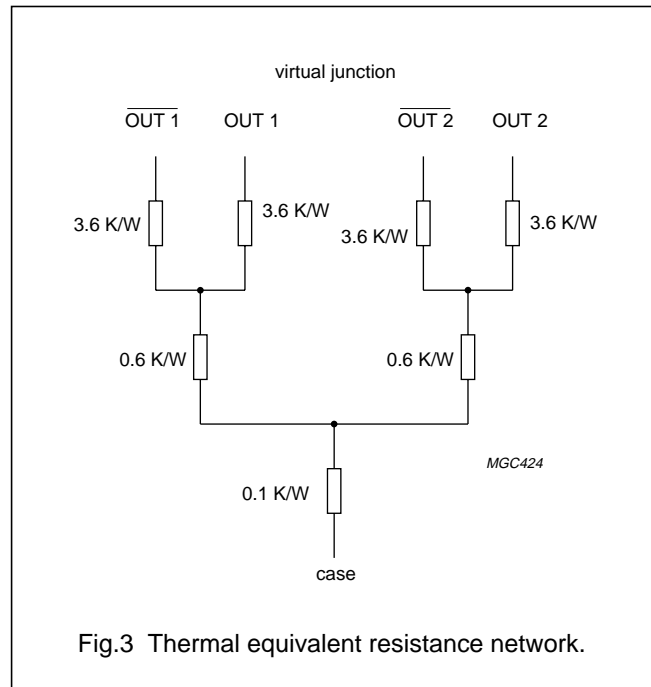
There are two parameters that determine the size of the heatsink. The first is the rating for the virtual junction temperature and the second is the ambient temperature at which the amplifier must still deliver its full power in the BTL mode.

With a conventional BTL amplifier, the maximum power dissipation with a music-like signal (at each amplifier) will be approximately two times 5 W. At a virtual junction temperature of 150 °C and a maximum ambient temperature of 60 °C, $R_{th(vj-c)} = 1.3 \text{ K/W}$ and $R_{th(c-h)} = 0.2 \text{ K/W}$, the thermal resistance of the heatsink

should be: $\frac{150 - 60}{2 \times 5} - 1.3 - 0.2 = 7.5 \text{ K/W}$

Compared to a conventional BTL amplifier, the TDA1561Q has a higher efficiency. The thermal resistance of the heatsink should be:

$1.7 \left(\frac{150 - 60}{2 \times 5} \right) - 1.3 - 0.2 = 13.8 \text{ K/W}$



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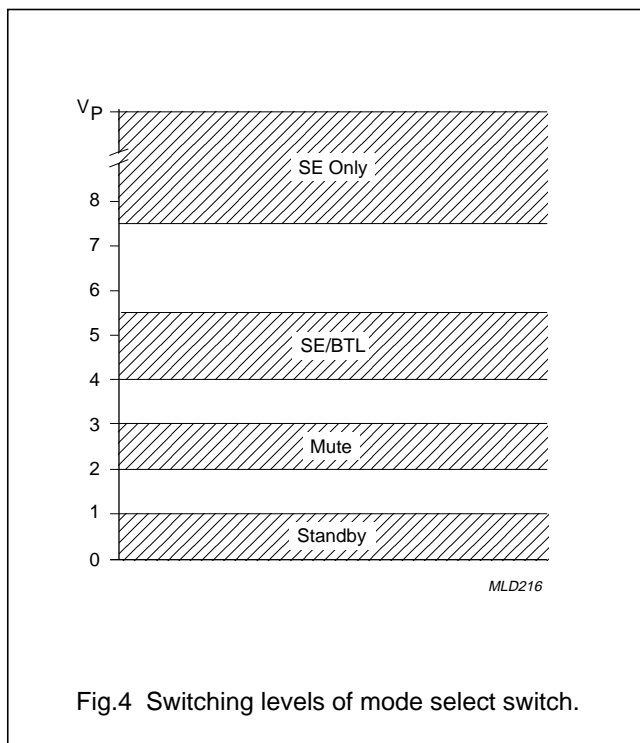
DC CHARACTERISTICS

$V_P = 14.4\text{ V}$; $T_{amb} = 25\text{ °C}$; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage	note 1	6.0	14.4	18.0	V
I_q	quiescent current	$R_L = \infty$	–	95	150	mA
I_{stb}	standby current		–	1	50	μA
V_C	average electrolytic capacitor voltage at pin 11		–	7.1	–	V
$ \Delta V_O $	DC output offset voltage	on state	–	–	150	mV
		mute state	–	–	50	mV
Mode select switch (see Fig.4)						
V_{ms}	voltage at mode select pin (pin 3)	standby condition	0	–	1	V
		mute condition	2	–	3	V
		on condition (SE/BTL mode)	4	–	5.5	V
		on condition (SE mode only)	7.5	–	V_P	V
I_{ms}	switch current through pin 3	$V_{ms} = 5\text{ V}$	–	–	40	μA
Protection						
T_{dis}	BTL disable temperature		–	145	–	$^{\circ}\text{C}$

Note

- The circuit is DC biased at $V_P = 6$ to 18 V and AC operating at $V_P = 8$ to 18 V .



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AC CHARACTERISTICS

$V_P = 14.4$ V; $R_L = 4$ Ω ; $C_{11} = 1000$ μ F; $f = 1$ kHz; $T_{amb} = 25$ °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 1%	15	18	–	W
		THD = 10%	21	23	–	W
		EIAJ	–	36	–	W
		$V_P = 13.2$ V; THD = 0.5%	–	14	–	W
		$V_P = 13.2$ V; THD = 10%	–	20	–	W
THD	total harmonic distortion	$P_o = 1$ W; $f = 1$ kHz; note 1	–	0.1	–	%
P_d	dissipated power		see Figs 9 and 10			W
B_p	power bandwidth	THD = 1%; $P_o = -1$ dB with respect to 15 W	–	20 to 15 000	–	Hz
$f_{ro(l)}$	low frequency roll-off	-1 dB; note 2	–	25	–	Hz
$f_{ro(h)}$	high frequency roll-off	-1 dB	130	–	–	kHz
G_v	closed loop voltage gain		31	32	33	dB
SVRR	supply voltage ripple rejection	$R_s = 0$ Ω ; $V_{ripple} = 2$ V (p-p) on; $f = 1$ kHz	45	60	–	dB
		mute; $f = 1$ kHz	–	90	–	dB
		standby; $f = 100$ Hz to 10 kHz	80	–	–	dB
CMRR	common mode rejection ratio	$R_s = 0$ Ω ; $f = 1$ kHz	–	80	–	dB
$ Z_i $	input impedance		45	60	75	k Ω
$ \Delta Z_i $	mismatch in input impedance		–	1	–	%
V_{SE-BTL}	SE to BTL switch voltage level	note 3	–	3	–	V
$ V_{out} $	output voltage-mute (RMS value)	$V_i = 1$ V (RMS)	–	50	100	μ V
$V_{n(o)}$	noise output voltage	on; $R_s = 0$ Ω ; note 4	–	160	300	μ V
		on; $R_s = 10$ k Ω ; note 4	–	170	–	μ V
		mute; note 5	–	20	–	μ V
α_{cs}	channel separation	$R_s = 0$ Ω	40	60	–	dB
$ \Delta G_v $	channel unbalance		–	–	1	dB

Notes

1. The distortion is measured with a bandwidth of 10 Hz to 30 kHz.
2. Frequency response externally fixed (input capacitors determine low frequency roll-off).
3. The SE to BTL switch voltage level depends on V_P .
4. Noise output voltage measured with a bandwidth of 20 Hz to 20 kHz.
5. Noise output voltage is independent of R_s (see Fig.6)($V_i = 0$ V).

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TEST AND APPLICATION INFORMATION

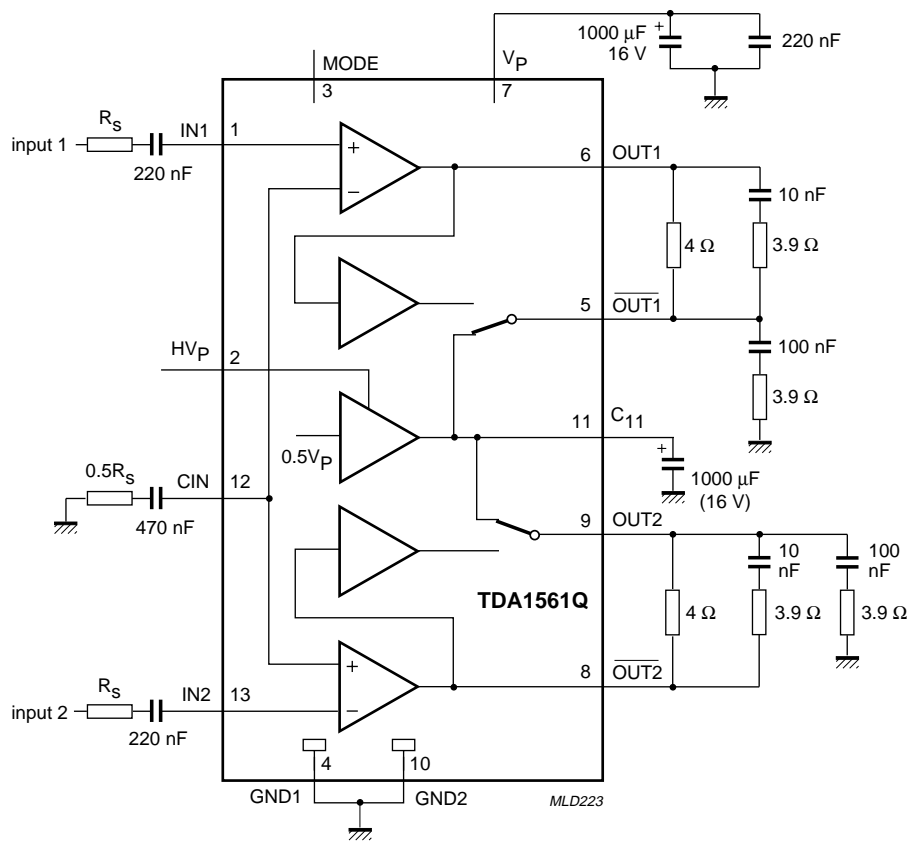
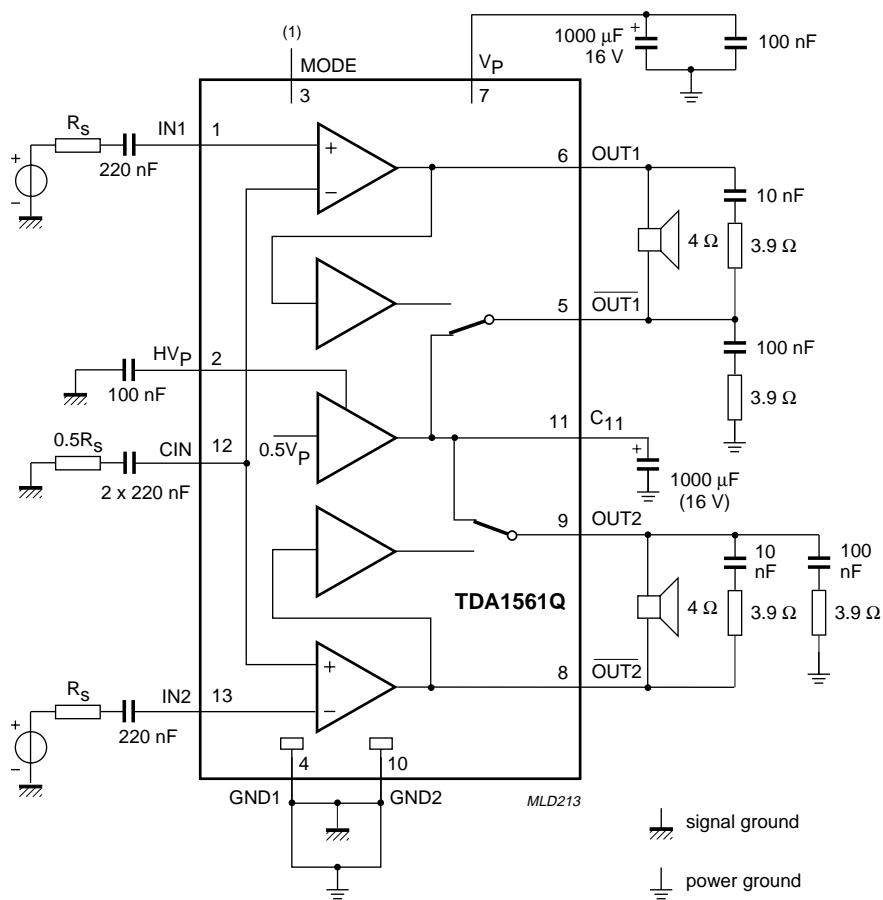


Fig.5 Test diagram.

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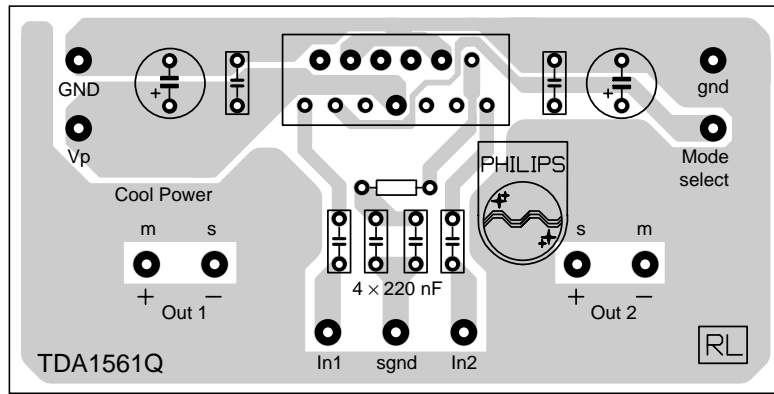
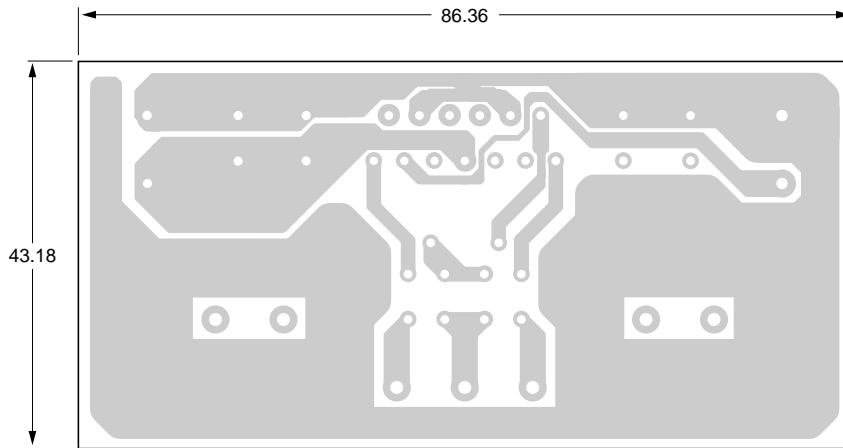


Connect Boucherot filter to pin 4 respectively pin 10 with the shortest possible connection.

Fig.6 Application diagram.

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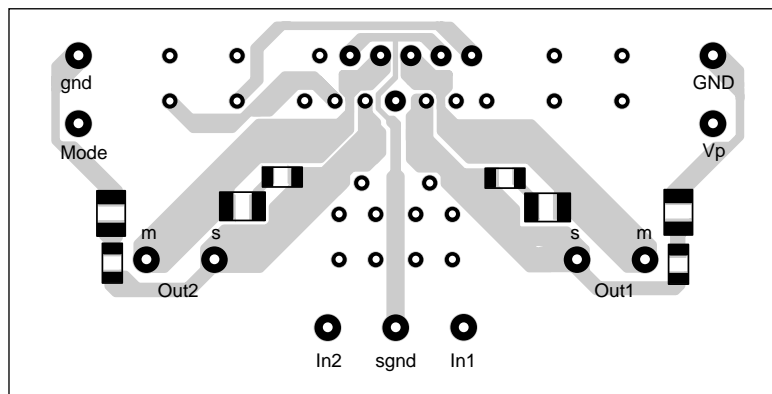
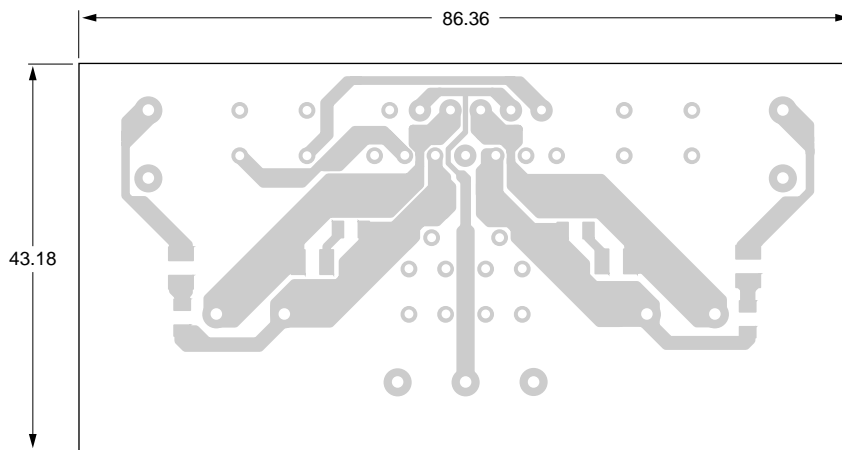
MGK182

Dimensions in mm.

Fig.7 PCB layout (component side) for the application of Fig.6.

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MGK183

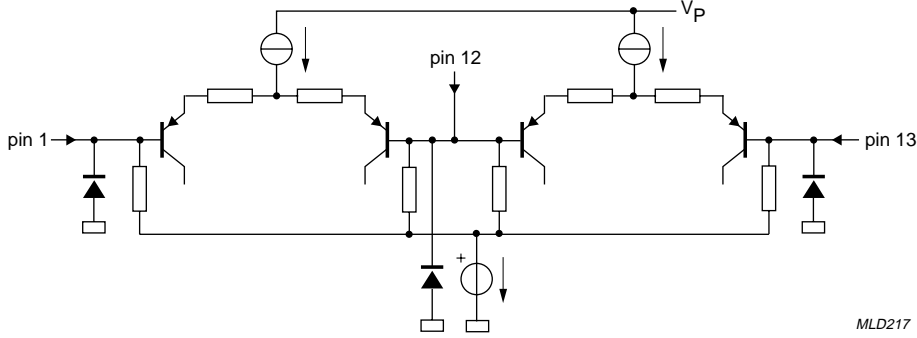
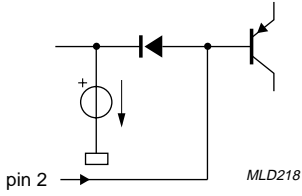
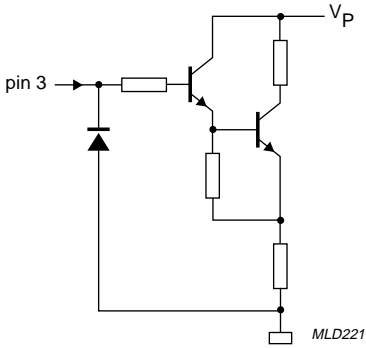
Dimensions in mm.

Fig.8 PCB layout (soldering side) for the application of Fig.6.

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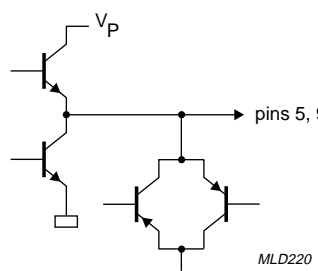
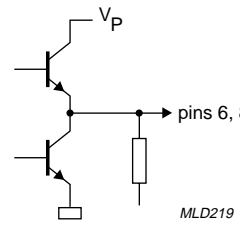
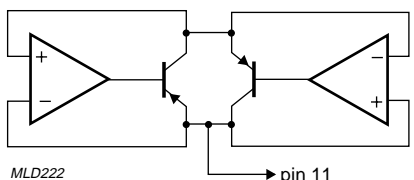
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INTERNAL PIN CONFIGURATIONS

PIN	NAME	EQUIVALENT CIRCUIT
1,12,13	IN1, CIN, IN2	 <p style="text-align: right;"><i>MLD217</i></p>
2	HV _P	 <p style="text-align: right;"><i>MLD218</i></p>
3	MODE	 <p style="text-align: right;"><i>MLD221</i></p>

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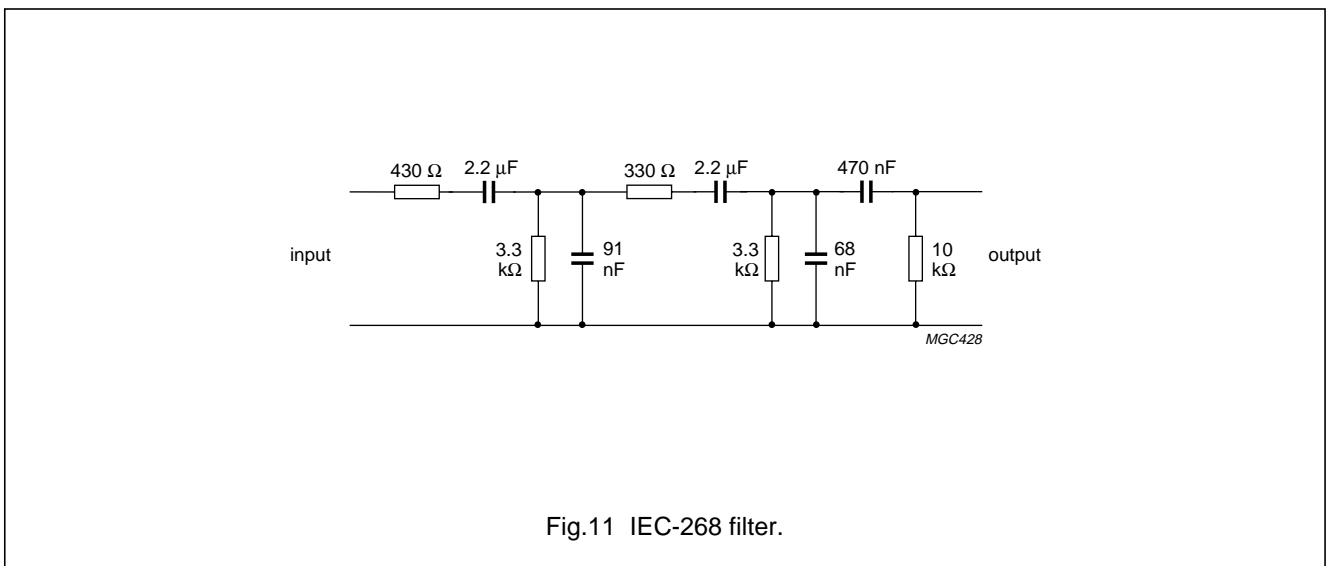
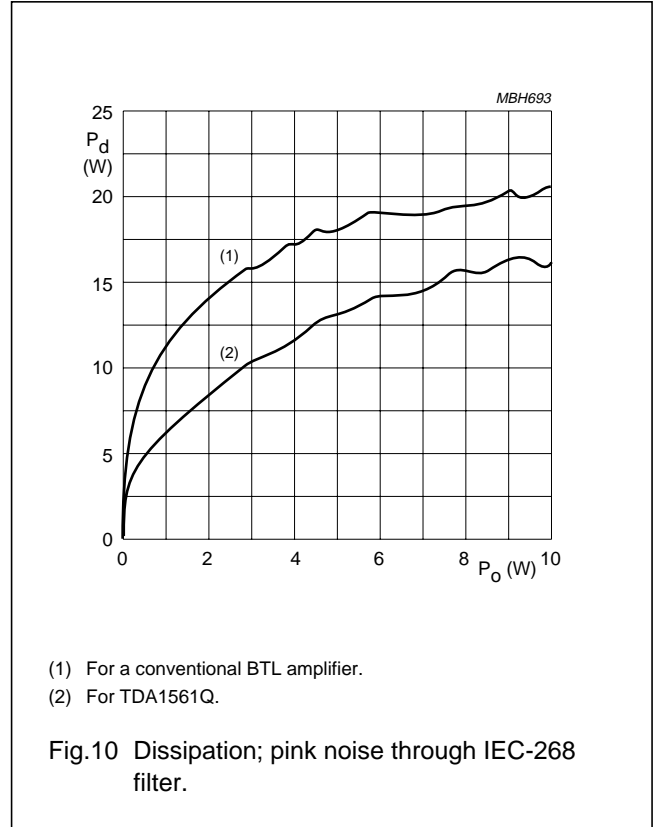
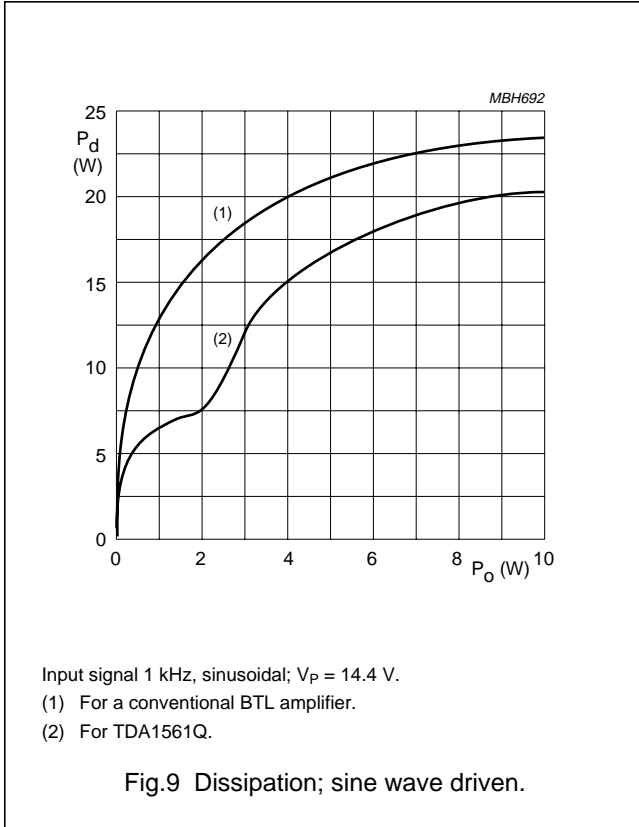
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PIN	NAME	EQUIVALENT CIRCUIT
5, 9	OUT1, OUT2	
6, 8	OUT1, OUT2	
11	C ₁₁	

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ADDITIONAL APPLICATION INFORMATION



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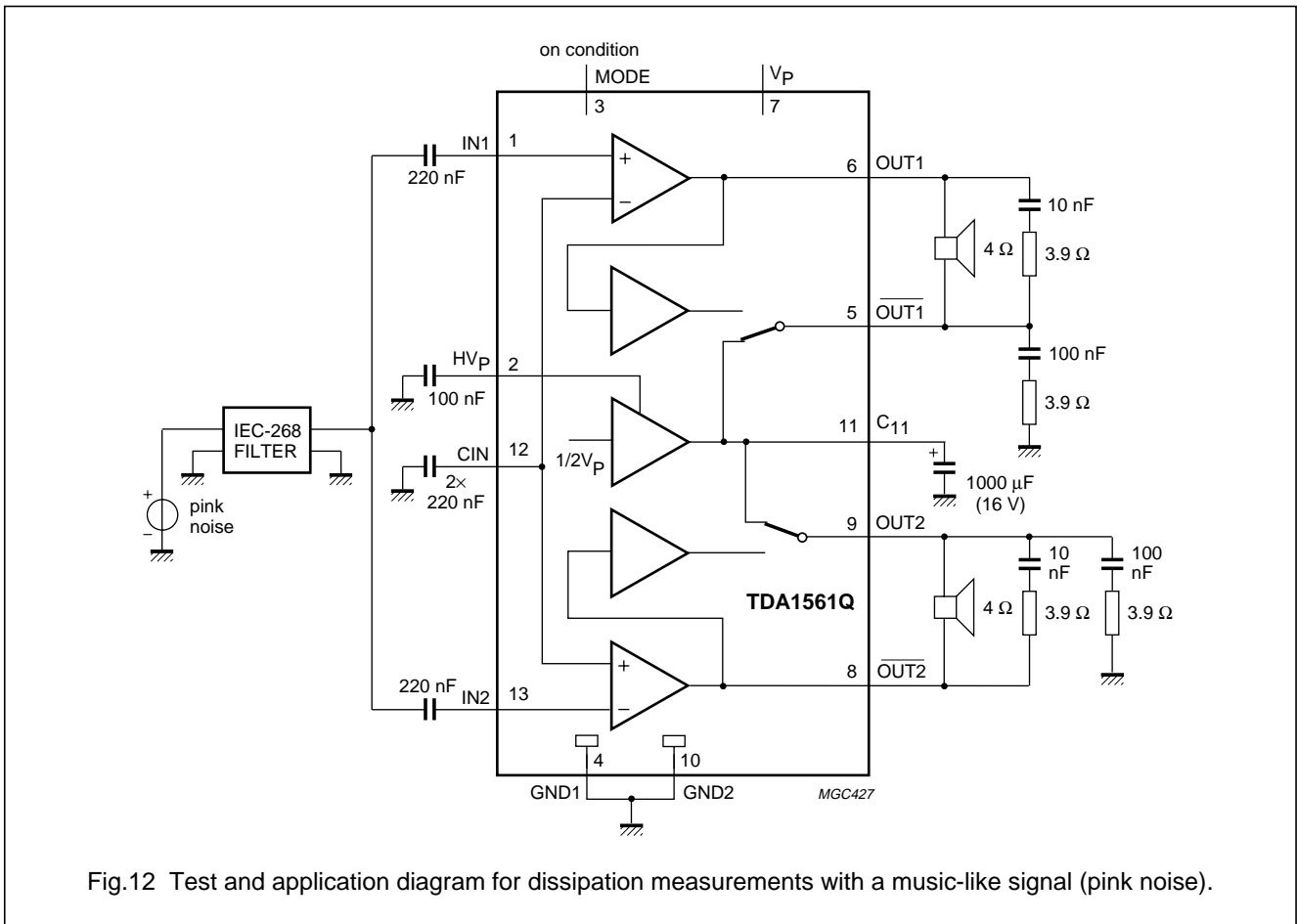


Fig.12 Test and application diagram for dissipation measurements with a music-like signal (pink noise).

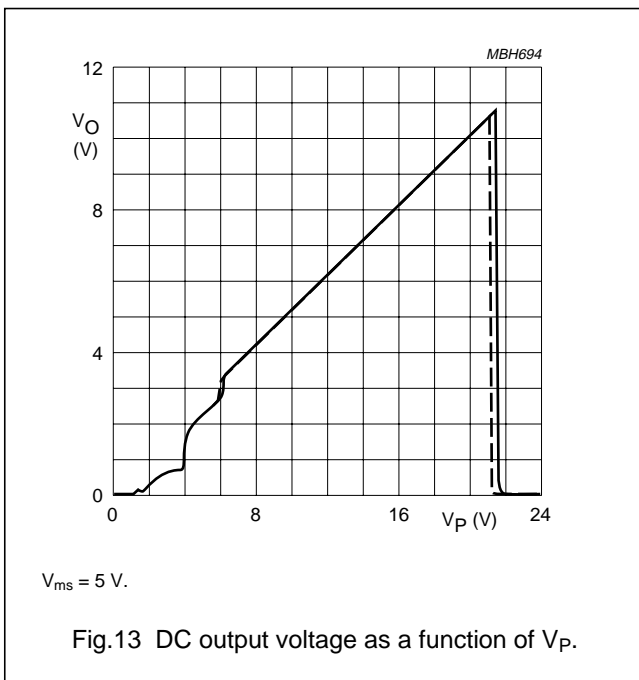


Fig.13 DC output voltage as a function of V_P .

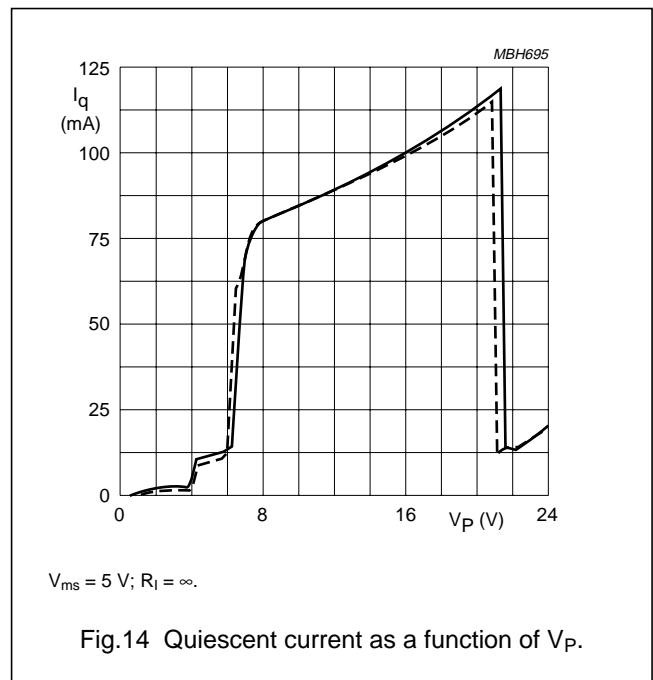
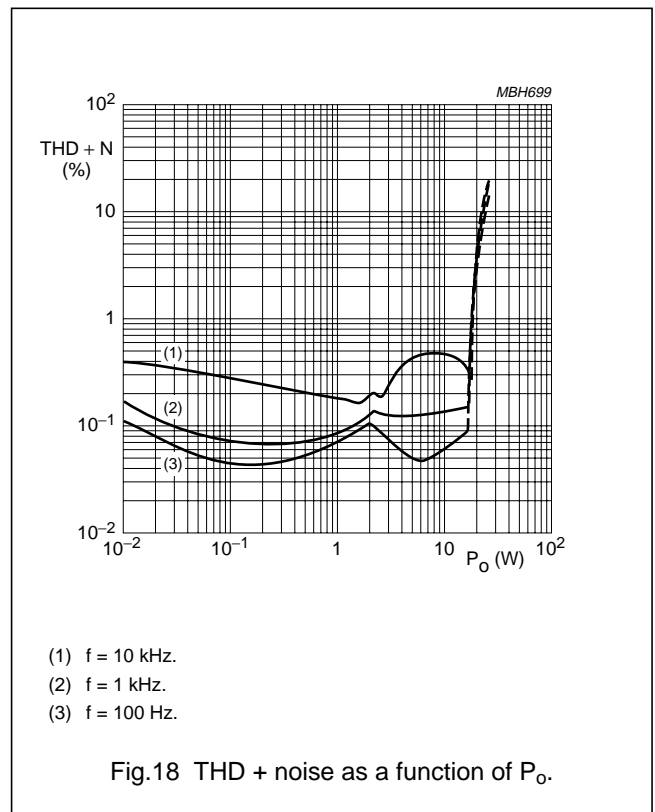
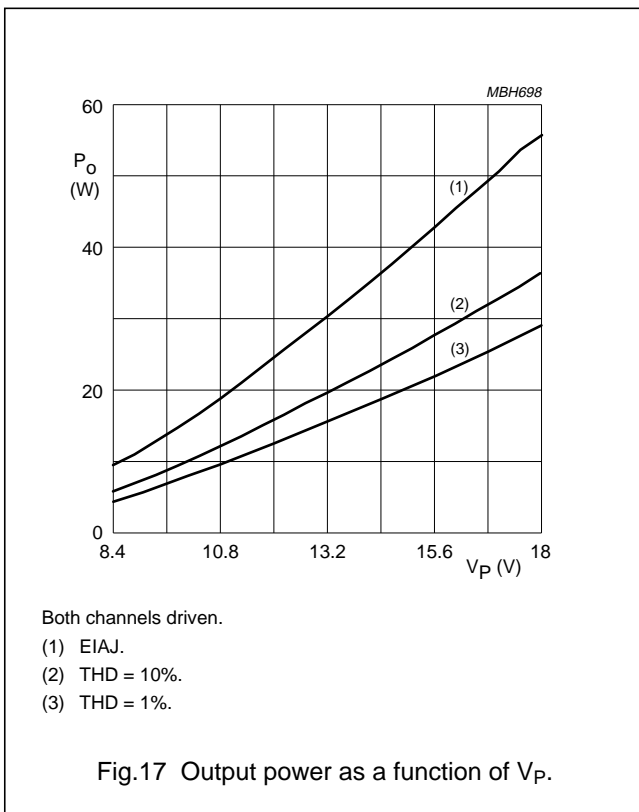
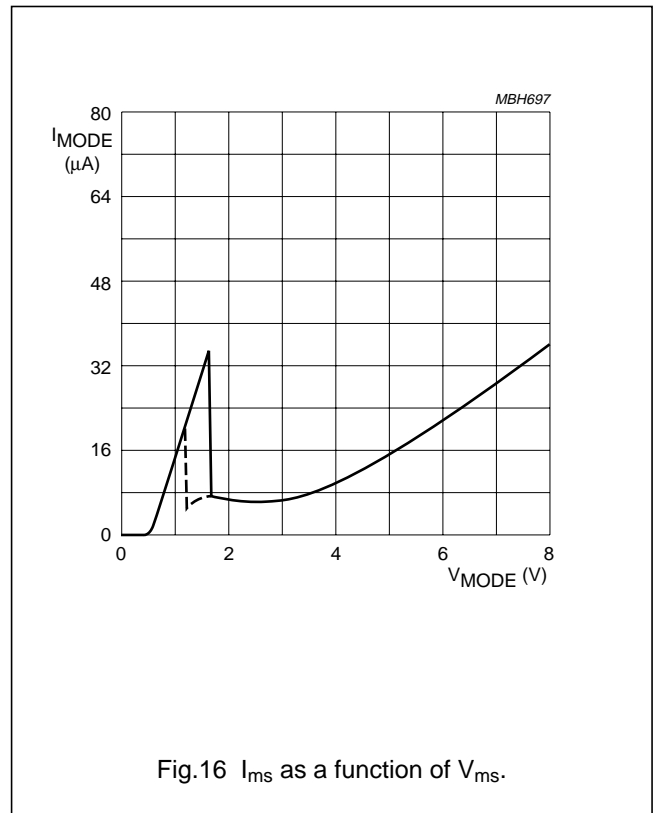
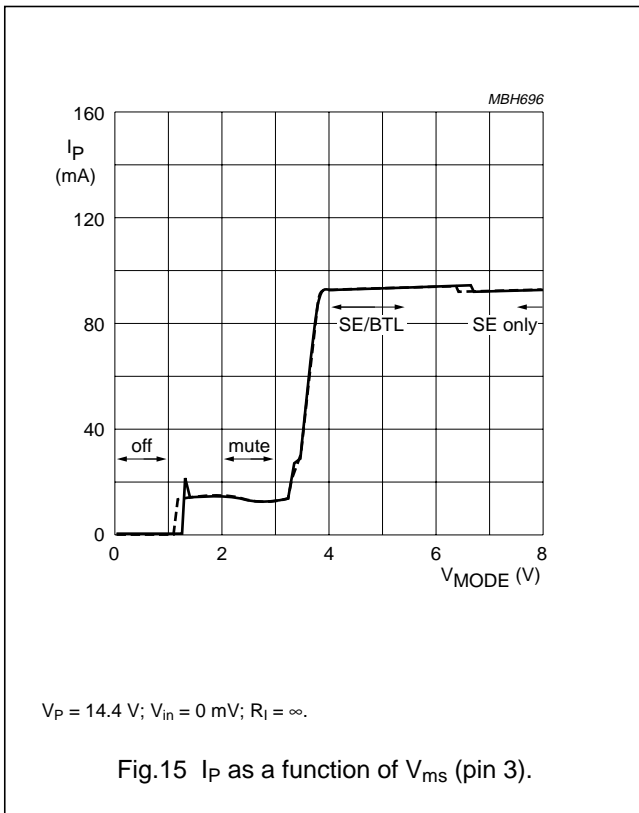


Fig.14 Quiescent current as a function of V_P .

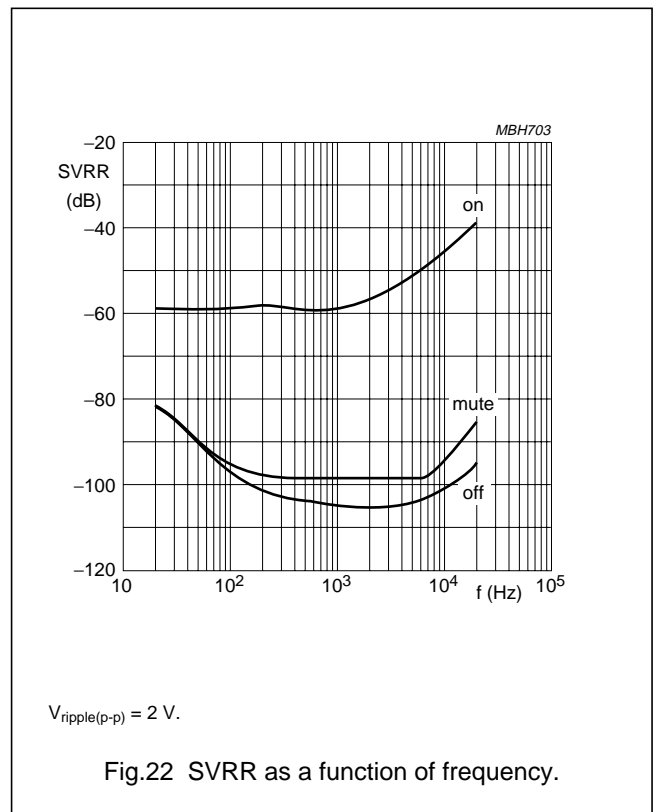
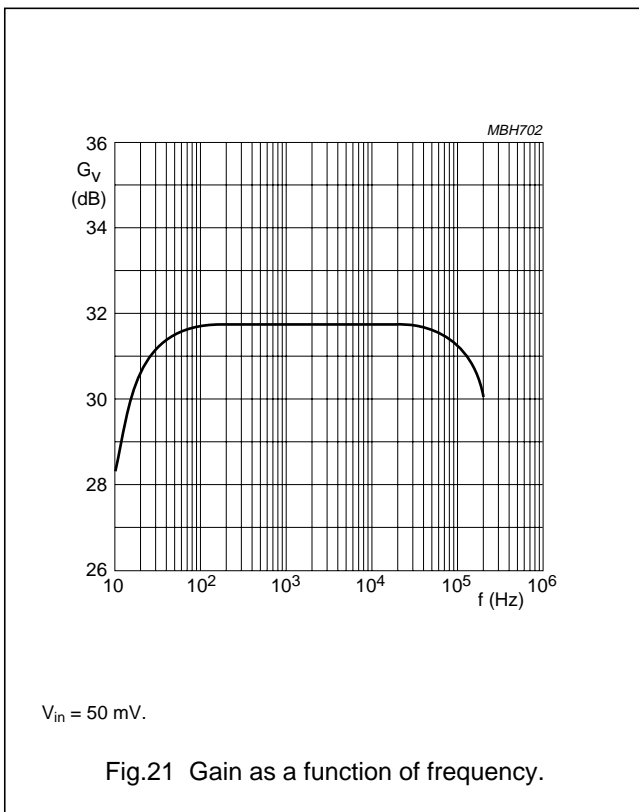
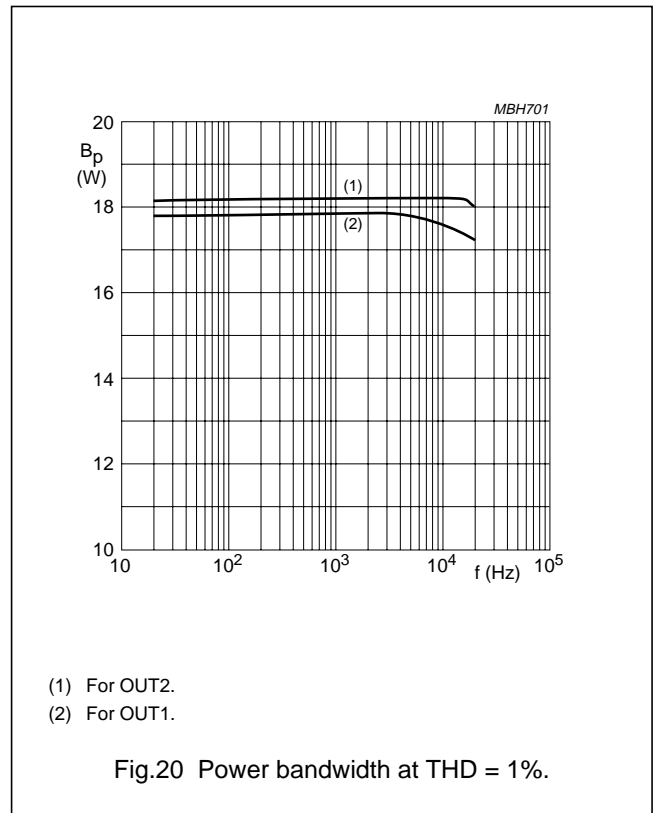
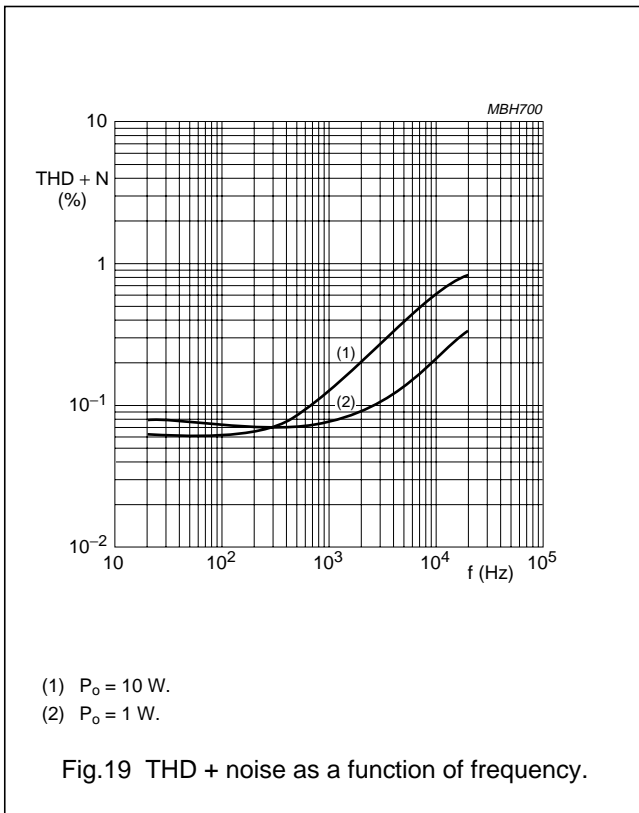
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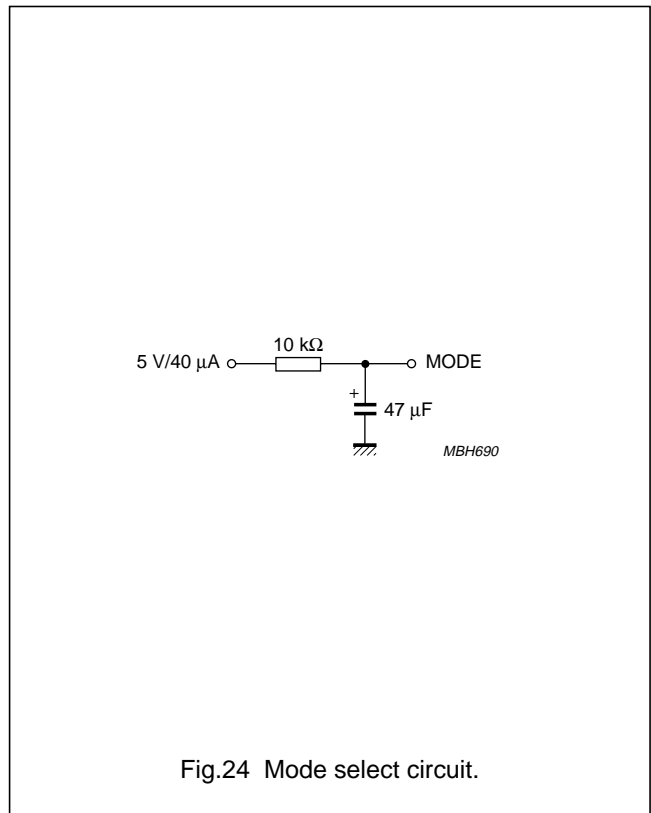
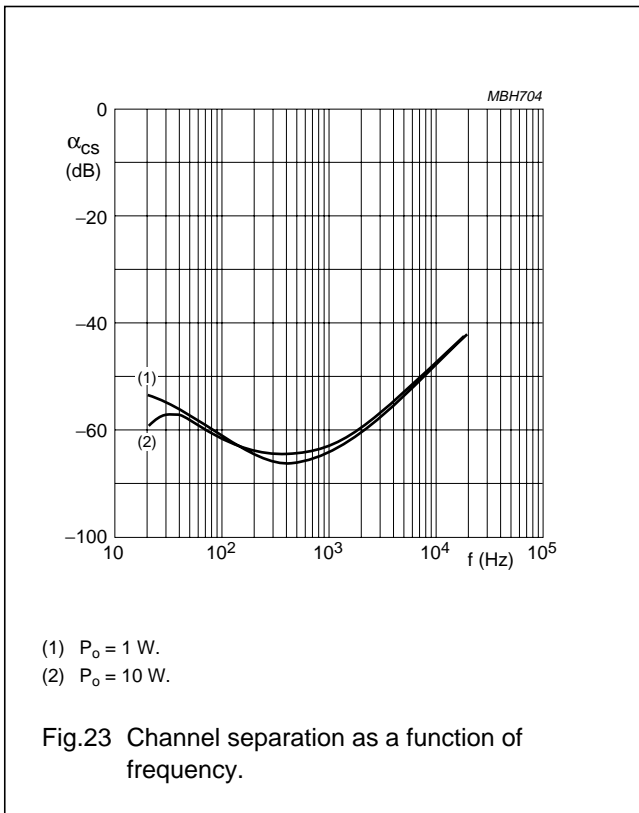
2 × 23 W high efficiency car radio power amplifier

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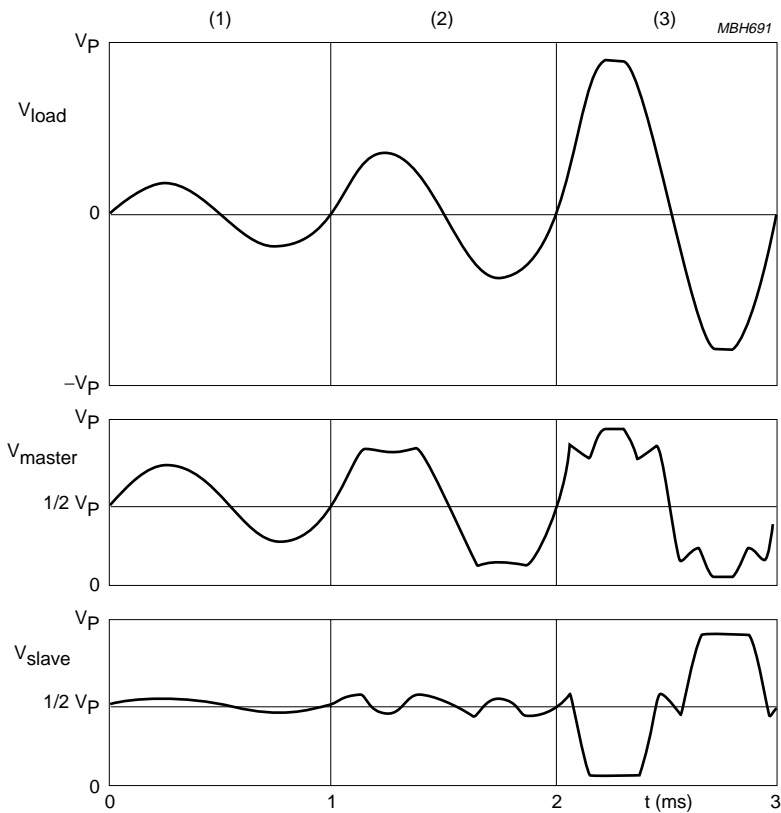
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2 × 23 W high efficiency car radio power amplifier

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See Fig.5:

$$V_{load} = V_6 - V_5 \text{ or } V_8 - V_9$$

$$V_{master} = V_6 \text{ or } V_8$$

$$V_{slave} = V_5 \text{ or } V_9$$

Fig.25 Output waveforms.

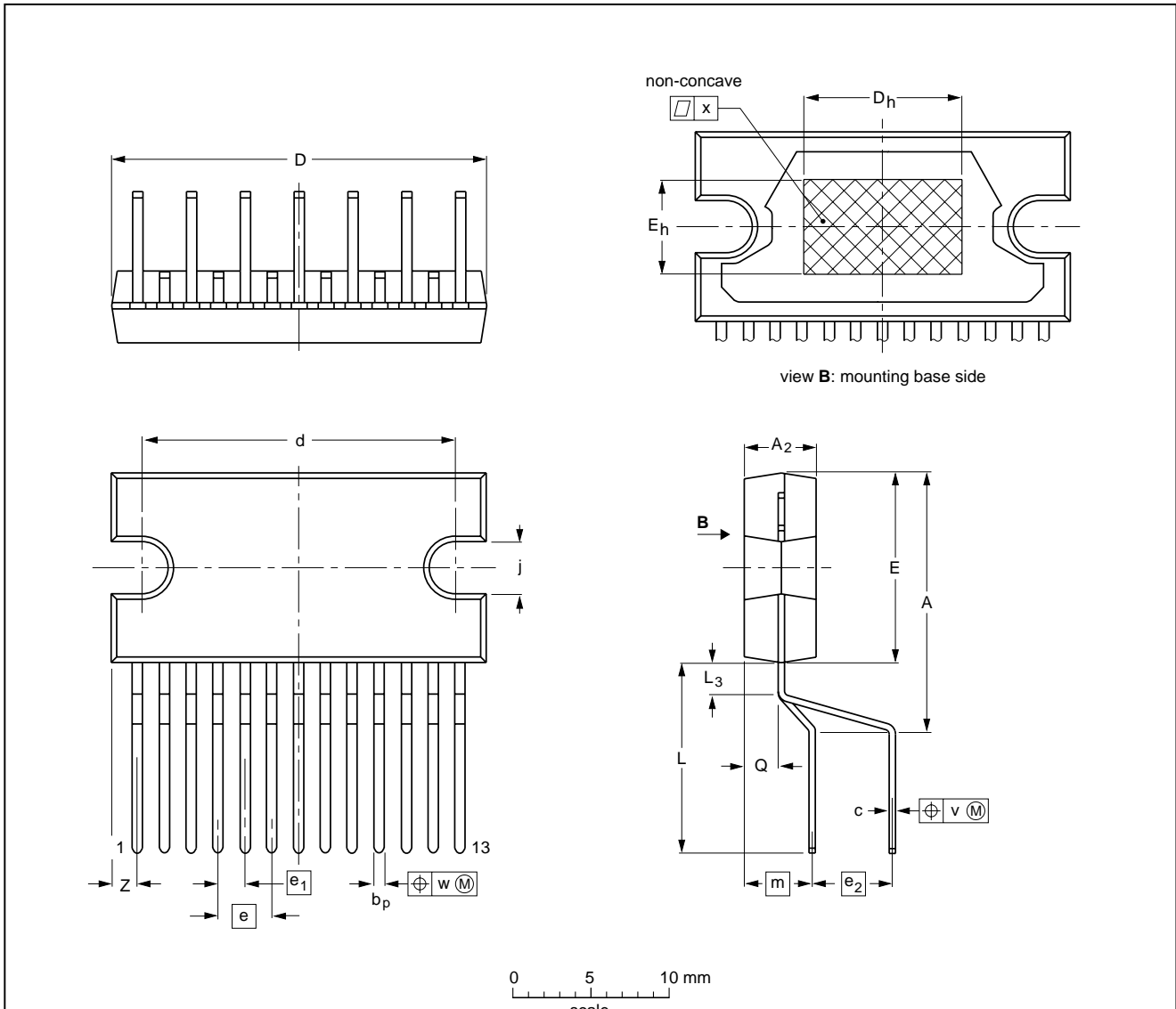
2 × 23 W high efficiency car radio power amplifier

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PACKAGE OUTLINE

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)

SOT141-6



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₂	b _p	c	D ⁽¹⁾	d	D _h	E ⁽¹⁾	e	e ₁	e ₂	E _h	j	L	L ₃	m	Q	v	w	x	z ⁽¹⁾
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT141-6						95-03-11 97-12-16

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax. +381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: <http://www.semiconductors.philips.com>

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Printed in The Netherlands

547027/1200/05/pp24

Date of release: 1997 Aug 14

Document order number: 9397 750 02732

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